University of Southern Queensland
Faculty of Engineering and Surveying

CURRENT CONTROLLER FOR INVERTER BRIDGE DESIGNED FOR GRID-CONNECTED PHOTOVOLTAIC SYSTEM

A dissertation submitted by

Alista Miletic

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ABSTRACT

A grid-connected photovoltaic system provides electrical energy to the power grid from power generated by a solar system. The first requirement in connecting to the power grid is converting the DC voltage generated by the photovoltaic cells to AC. This is achieved using a single-phase switch-mode inverter. The next requirements are that the output frequency matches that of the grid to which it is connected and its current is near sinusoidal. Power supply authorities set stringent standards that limit the amount of DC delivered to the grid and therefore the inverter must be controlled to minimise the DC content of the sinusoidal output. To produce this waveform, the inverter is operated in unipolar mode and controlled using sinusoidal pulse-width modulation. This task is performed by a current controller circuit that controls the inverter output current by regulating the inverter transistor switching using tolerance band control.

A current controller circuit using standard ICs and discrete electronic components had previously been designed for a switch-mode inverter. The objectives of this project were to prove the existing current controller design for correct and suitable operation and to research the possibility of optimising it by implementation using modern technology such as PIC microcontrollers.

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Alista Miletic
Student Number: Q12209622

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Chapter 1 INTRODUCTION

1.1 Background Information

A grid-connected photovoltaic system is a system designed to supply the power grid with electrical energy generated by photovoltaic cells. The complete photovoltaic system is comprised of a number of smaller systems, such as the photovoltaic panels, DC to DC converter, maximum power tracker, current controller and inverter. Because of the complexity of the system, the area of research for this project was limited to the current controller, gate drive circuit and switch-mode inverter. This section, as illustrated in figure 1.1, is referred to as the current controller system.

The purpose of the current controller system is to connect the solar generated power to the power grid. This requires AC conversion of the DC power supplied to the inverter so that its output frequency matches that of the grid to which it is connected. By including inductance in the inverter load and increasing the transistor switching frequency by approximately 100 times the output frequency, the output current is regulated to produce a sinusoidal waveform with minimal DC content. To achieve this, the inverter is operated in unipolar mode and controlled using sinusoidal pulse-width modulation. This task is performed by a current controller circuit which regulates switching of the inverter transistors to keep the difference between the inverter output current waveform and desired waveform within a predetermined value. This current control method, referred to as the tolerance band control technique, allows full control of the ripple content of the inverter output waveform.

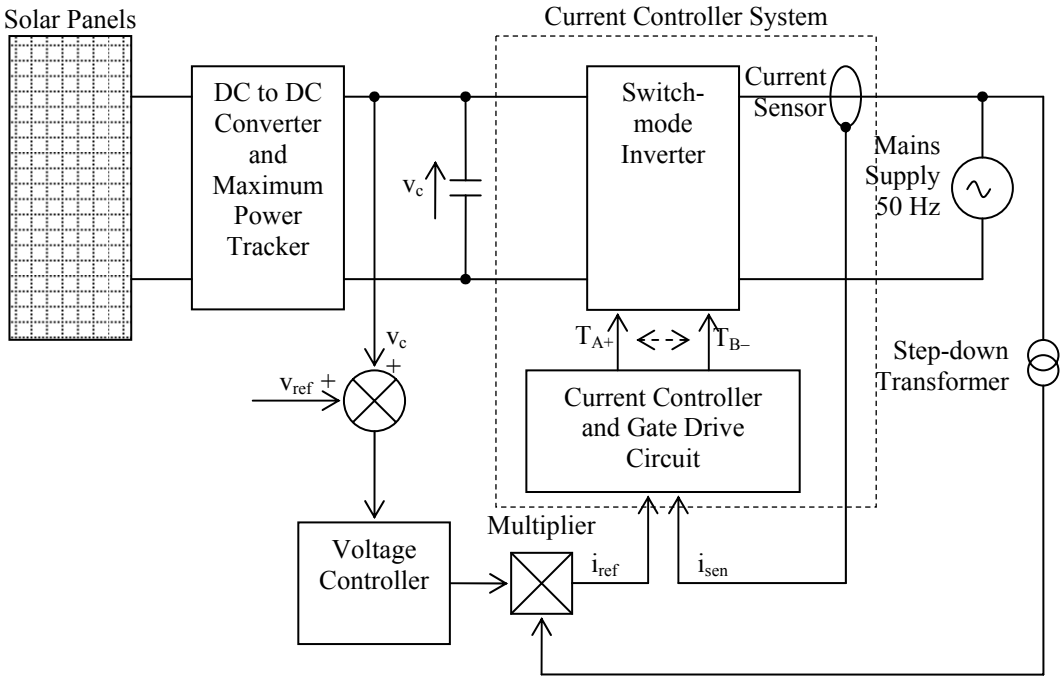


Figure 1.1: Photovoltaic System Block Diagram.

1.2 Project Objectives

A current controller circuit for the photovoltaic system was previously designed using standard ICs and discrete electronic components. In an attempt to reduce future manufacturing and material costs, it was anticipated that the existing electronics could be replaced by a single chip device. The preferred device for this task was a PIC microcontroller.

Improving the existing current controller by implementation of modern technology required research into PIC microcontrollers but this project also included researching the various components of the current controller system. This included switch-mode inverters, current control techniques, optocouplers and gate drive circuits. The activities involved in this project were to temporarily construct and test the original current controller system for correct and suitable operation, and to design and build printed circuit boards (PCBs) of the original current controller circuit.

The project specifications put forward at the start of this thesis were as follows.

1. Temporarily construct and prove the existing current controller circuit.
2. Research the possibility of replacing the standard IC's with PIC microcontrollers or Digital Signal Processors (DSPs) if the PICs proved to be unsuitable.
3. Replace the temporary current controller components with the new PICs or DSPs and make the necessary adjustment required to achieve the desired output.
4. Design a PCB layout on the new circuit once it has be tested and proven.
5. Construct the final circuit board and test.

1.3 Dissertation Outline

The first chapter of this dissertation provides an overview of a grid-connected photovoltaic system and explores the fundamental components that make up the current controller system.

Chapter 3 outlines some of the applications and types of switch-mode inverter circuits available and provides a detailed analysis of the single-phase square-wave bridge inverter. This chapter also includes sections on bipolar and unipolar sinusoidal pulse-width modulation control techniques and concludes with the harmonic content of the unipolar control method.

Chapter 4 outlines the basic principles behind common modulation techniques that are used to regulate the inverter transistor switching. The chapter concludes with a detailed analysis of the tolerance band current control technique implemented by the photovoltaic system.

Chapter 5 deals with the issue of implementing the current controller into the photovoltaic system. This includes an operational explanation of the original current controller circuit, and the gate drivers and optocouplers required to interface the current controller with the inverter.

Chapter 6 outlines the steps involved in testing each section of the current controller system including the results obtained. Vital timing conditions and results are illustrated with oscilloscope images for various stages of the current controller, gate drive circuit and inverter transistors.

Chapter 7 concludes the dissertation with the outcome of the PIC microcontroller research. This includes an introduction to PIC microcontrollers, PIC requirements for current controller implementation and a detailed description and sample code of the suggested PIC18C242 chip.

Chapter 2 CURRENT CONTROLLER SYSTEM OVERVIEW

This chapter outlines the primary function of a grid-connected system and how it is implemented to supply a free source of energy to the power grid. The chapter also includes an overview of the fundamental components that make up the current controller system. This includes the basic principle of operation of the current controller circuit, optocouplers, gate drive circuit and inverter, and how each is integrated into the system.

2.1 The Grid-connected Photovoltaic System

A photovoltaic system converts radiant energy from the sun into electrical energy. A grid-connected system supplies this energy into the main power grid, providing a free source of renewable energy. Figure 2.1 illustrates the basic principle of the grid-connected photovoltaic system. It demonstrates DC power generated by photovoltaic or solar cells that are exposed to the sun. This power is converted to AC and then connected to the grid.

Inverting the DC to AC is a much greater challenge than converting AC to DC, and when connecting to the power grid there are many variables that need to be controlled. These are that the voltage amplitude and frequency must match the grid source and the waveform must be near sinusoidal with minimal DC content. For this project, these requirements were achieved by the use of a current controlled single-phase bridge inverter.

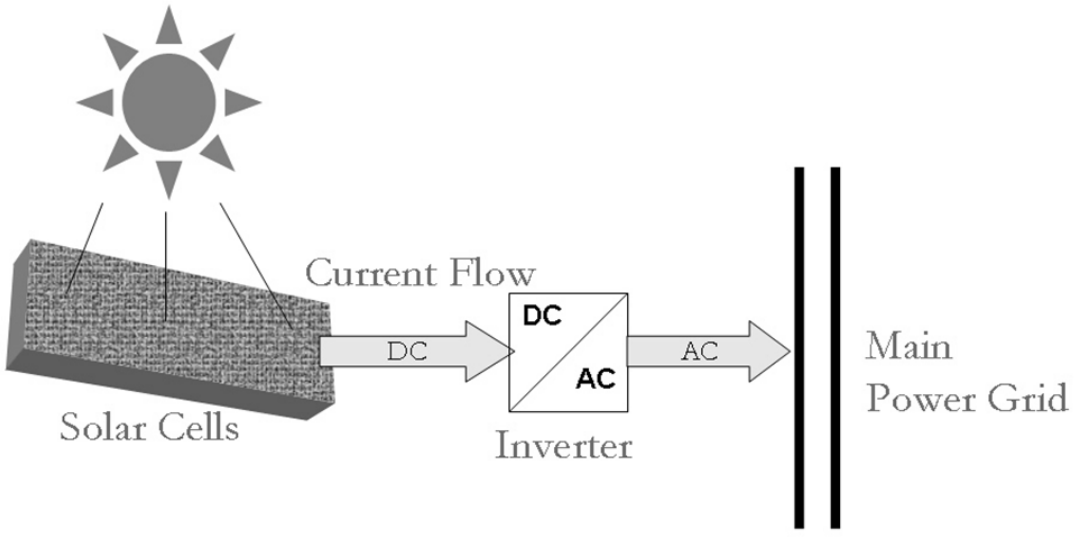


Figure 2.1: Illustration of a Grid-connected Photovoltaic System.

2.2 Current Controller System Overview

The current controller system consists of the current controller, optocouplers, gate drivers, bridge inverter and a current sensor. The system block diagram is illustrated in figure 2.2 and a description of the basic principle of operation is as follows.

The control circuit begins with a reference current input to the current controller, which in the final system will be a sample of the grid supply. The current controller is also supplied with an adjustable tolerance input that sets the magnitude of the tolerance band. To close the loop, a negative feedback current is supplied by a hall-effect sensor that monitors the inverter output current. The output of the controller provides the gate signals for the inverter transistors but this signal first passes through optocouplers to electrically isolate the current controller from the inverter. To ensure successful gate turn on, gate drive circuits are required to provide the higher currents required by the gates of the transistors. The gate drive circuit is controlled by the current controller output signal. The inverter transistors provide the switching interface between the control circuit and power circuit.

The power circuit begins by supplying the inverter rails with the DC voltage generated by the solar panels. Controlling of the transistors in the inverter bridge circuit regulates the load voltage to produce a sinusoidal AC output current. This output is directly connected to the power grid to provide a free source of electrical energy.

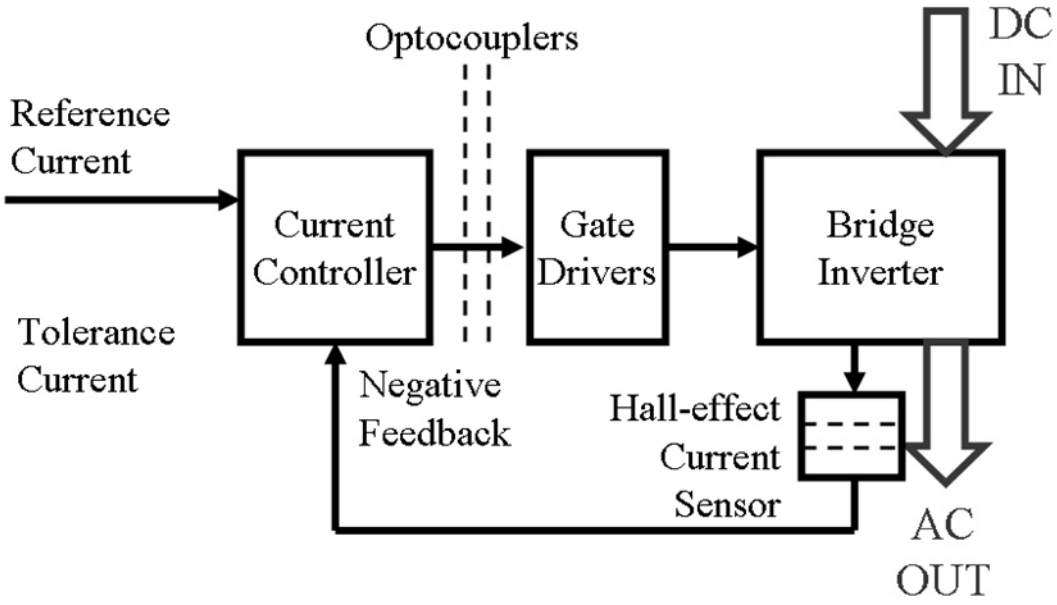


Figure 2.2: Current Controller System Block Diagram.

Chapter 3 SWITCH-MODE INVERTERS

To connect the DC voltage generated from the photovoltaic system to the main power grid, the DC must be inverted to AC. This process is achieved by a common inverter circuit. A simple inverter will oscillate the DC source from positive to negative at its output at a set frequency. Basic inversion produces a square-wave output but techniques can be implemented to control the shape of the output waveform. A switch-mode inverter is a power electronic circuit that provides these control capabilities and allow the output waveform to be shaped as desired.

The grid-connected circuit required the inverter output to match the sinusoidal grid voltage with minimal DC content. By employing a switch-mode inverter into the photovoltaic system and using pulse-width modulation control to regulate the transistor switching, the output current could be controlled to match that of the grid to which it was connected.

This chapter outlines some of the applications and types of switch-mode inverter circuits available including an in depth look at the single-phase square-wave bridge inverter. It continues with a detailed analysis of the bipolar and unipolar sinusoidal pulse-width modulation control techniques and concludes with the harmonic content of the unipolar control method.

3.1 Applications for Switch-mode Inverters

In electronic systems it is often required to convert alternating currents to direct currents with the process being quite simple. The simplest example of this would be a single diode in series with a sinusoidal AC source where the diode only allows current to flow in one direction and therefore only one half of each AC cycle passes through, thus producing a DC output. Filtering the DC output can also be a simple task where a simple filtering capacitor might be suitable. Contrary to AC to DC conversion, it is also common to have to convert direct current sources to alternating currents. This inversion is more complicated than AC to DC conversion because the output waveform often has to be controlled to a specific shape and frequency. For this reason, the electronics involved become more intricate and more components are required. Feedback systems are usually required to monitor and control the output to provide the desired waveform. Common inverter circuits that control the switching of the DC to produce AC outputs are switch-mode inverters.

Switch-mode inverters produce AC by alternating the output from positive to negative at the desired frequency. This often requires switching speeds to vary from 50 to many thousands of times per second. In most power electronic applications, the inverter circuits are also required to handle high currents. To handle these conditions, solid state silicon devices such as IGBTs, MOSFETs and BJTs are commonly used to do the switching (Mohan et al. 1985). IGBTs feature lower on-state switching losses compared to MOSFETs and have higher reverse blocking capabilities and lower base current requirements compared to BJTs. For these reasons, IGBTs were the chosen device used in the photovoltaic switch-mode inverter.

The applications of switch-mode inverters generally fall into the category of either motor control or non-motor control (Lander 1987). The basic differences between the two are variable or fixed output frequency. Motor control inverters, also referred to as AC adjustable speed drives, control the speed of AC motors by varying the output frequency. These drives can also adjust the motor torque by controlling the RMS voltage applied to the motor windings.

The constant frequency inverter is most commonly used as a standby power supply which provides an emergency power source at mains frequency in the event of mains failure. These inverter systems generally have a battery bank to provide a voltage source to the inverter during mains failure. There are two ways in which standby inverters are implemented, either to go online in the event of power failure for less critical situations, or to constantly supply power to the load and only use the mains power to keep the battery bank charged. The former system would introduce a delay between change-over while the latter provides a true uninterruptible supply and would be used in critical situations such as life support machines in hospitals.

Aside from the two most common inverter applications there are also more specific uses for switch-mode inverters such as providing power to the main grid which is the objective of this project.

3.2 Types of Switch-mode Inverters

The input to switch-mode inverters are most commonly supplied by a constant DC source and are referred to as voltage source inverters or VSIs (Mohan et al. 1985). This is the case for the photovoltaic system where the DC voltage is supplied by the solar panels. The other less common inverter is the current source inverter or CSI and is only used for very high power AC motor drives (Mohan et al. 1985).

The two most common VSIs are the square-wave and pulse-width modulation inverters. Conventionally, both have the same circuitry but differ by their supply voltage with the square-wave inverter having a variable DC supply and the PWM inverter having a constant DC supply.

The single-phase square-wave bridge inverter produces a square-wave output voltage. A purely resistive load will produce a square-wave current in phase with the voltage. This waveform changes instantaneously at its edges but the PWM technique requires this current to have a steady rise and fall time. The inclusion of inductance in the load achieves this by producing an exponential change of current and also results in reducing the magnitude of the output harmonics.

For situations where the DC input voltage is constant, the PWM inverter is preferred because it controls both the output frequency and the RMS output voltage. With a fixed inverter rail voltage, the magnitude of the voltage output is constant but the RMS value can be varied by controlling the mark to space ratio of the inverter switching.

Modifications can be made to single-phase bridge inverters to produce three-phase outputs. It is possible to supply a three-phase load by means of three separate single-phase inverters with the output displaced 120° from each other. Three-phase switch-mode inverters are very common because they form the basis of variable speed drives which are used extensively in industry.

There are various other switch-mode inverters such as the push-pull single-phase inverter. This circuit has the advantage of having half the required switches but the disadvantage of requiring a centre tapped transformer. With the photovoltaic system being designed to be compact and relatively inexpensive, the inclusion of a transformer was not desirable and therefore the preferred device to perform the DC to AC conversion was the square-wave bridge inverter.

3.3 Operation of Single-phase Square-wave Bridge Inverter

A single-phase square-wave bridge inverter circuit is displayed in figure 3.1. It shows four switches T_{A+}, T_{B+}, T_{A-} and T_{B-} and feedback diodes D_{A+} to D_{B-} connected to an inductive load. The photovoltaic system incorporates IGBTs with inbuilt feedback diodes for these devices. This inverter circuit can control the output voltage polarity and current direction independently. This is referred to as four quadrant operation. The inverter load voltages and currents for a complete cycle are illustrated in figure 3.2. The figure also illustrates typical current patterns for each branch of the inverter circuit including the base currents of the 4 transistors. Basic operation of the inverter is as follows.

Starting with transistors T_{A+} and T_{B-} on; the load voltage is equal to the DC voltage E and the current rises exponentially. At half the full cycle T_{A+} and T_{B-} are de-energised and T_{B+} and T_{A-} are turned on. This reverses the voltage across the load but the inductive load prevents the current from reversing instantaneously. Instead, the load current decreases exponentially through the feedback diodes D_{B+} and D_{A-} until it reaches zero and then starts to flow in the reverse direction through transistors T_{B+} and T_{A-}. In the situations when load current flows through the feedback diodes, power is being delivered back to the DC source by the inverter. Once the full cycle is reached, T_{B+} and T_{A-} are de-energised and T_{A+} and T_{B-} are turned back on which forces the load current to flow through the feedback diodes D_A+ and D_B- until the zero crossing. An important factor that must be addressed is that at no instance can the same side transistors, i.e. T_{A+} and T_{A-} or T_{B+} and T_{B-}, be energised simultaneously because this would result in shorting the DC supply rails. This process completes one cycle and is repeated at the desired frequency which is determined by the switching periods of the transistors.

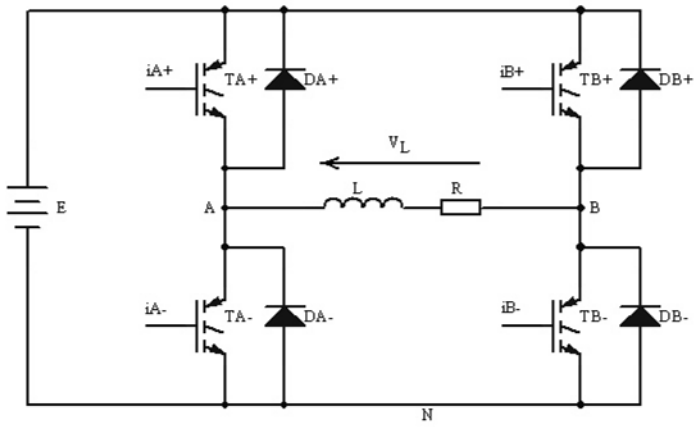


Figure 3.1: Single-phase Square-wave Bridge Inverter.

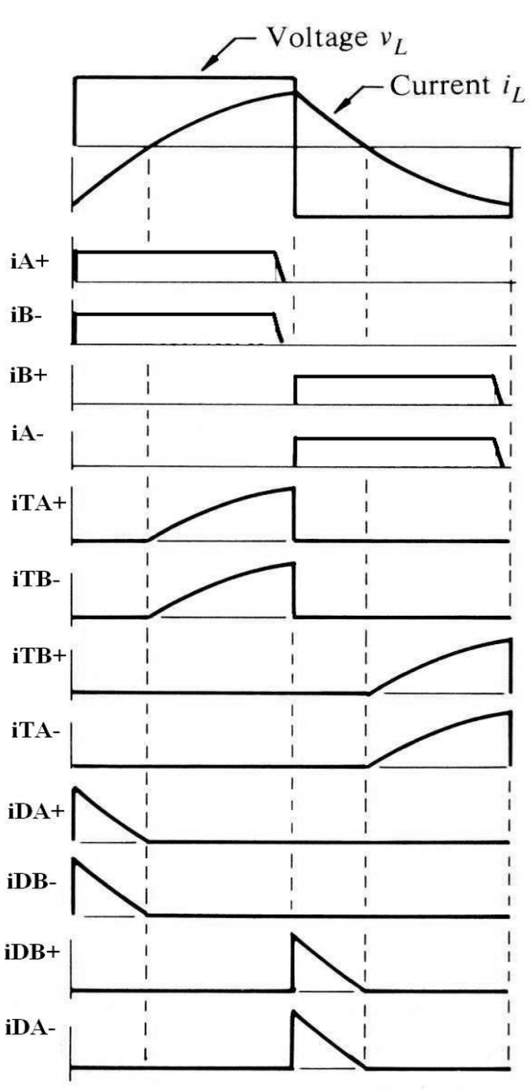


Figure 3.2: Square-wave Output (Lander 1987, p184).

Although basic operation of the bridge inverter can control the output frequency it cannot control the magnitude of the voltage. Varying the rms output voltage can be achieved by one of the following techniques.

- **Controlling the DC supply voltage.**
  The inverter output voltage can be adjusted by controlling the voltage applied to the DC supply rails. This is a simple approach but in practice the ability to vary the DC isn't always available or efficient and therefore seldom used in practice. The photovoltaic cells produce a constant DC supply and therefore another method of voltage control would be required.

- **Voltage cancellation.**
  By introducing zero periods of voltages into the square-wave, the rms voltage can be reduced. This alters the current pattern because the rate of change of current for an inductor is proportional to the magnitude of the voltage. Therefore the rate of change in load current will be less during the periods where there is zero voltage across the load. The resulting waveform is known as a quasi-square-wave (Lander 1987). Although this technique varies the rms voltage, it does not give good control of the output current waveform. For this reason, a better method was desirable in the photovoltaic system.

- **Pulse-width modulation.**
  The mark to space ratio of the inverter output voltage is controlled to regulate the rms voltage output and the current waveform (Mohan et al. 1985). This technique controls the transistor switching periods by comparing a carrier signal to a modulating signal. The photovoltaic system uses sinusoidal PWM control to produce an output current that matches the sinusoidal waveform of the grid supply. This method can be implemented using either bipolar or unipolar control. Both of these schemes are analyses in the following sections.

3.4 Bipolar Sinusoidal PWM Control

Sinusoidal PWM to compares a carrier signal known as the triangular signal v_{tri} with a sinusoidal signal known as the modulating or control signal $v_{control}$. This section outlines the basic principle of bipolar operation.

Bipolar sinusoidal PWM control allows the instantaneous load voltage v_L to be either positive or negative during both cycles of $v_{control}$ as illustrated in figure 3.3. This control process works by energising T_{A+} and T_{B-} while $v_{control}$ is greater than v_{tri} and T_{B+} and T_{A-} while $v_{control}$ is less than v_{tri}. The transistor switching strategy with respect to $v_{control}$ and v_{tri} is further simplified in table 3.1.

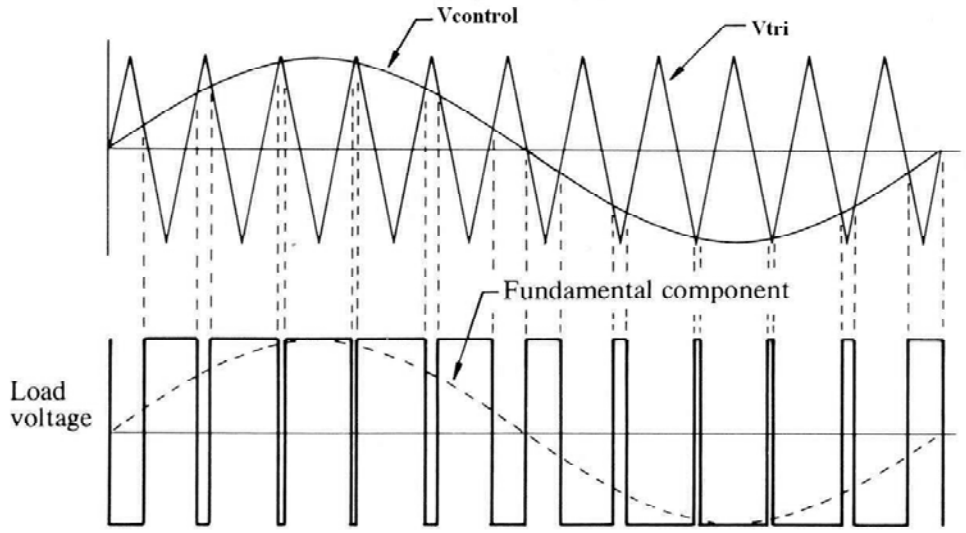


Figure 3.3: Bipolar Sinusoidal PWM Waveforms (Lander 1987).

Table 3.1: Transistor Switching Strategy (Bipolar).

Transistor	T_{A+}	T_{B-}	T_{B+}	T_{A-}	v_L
$v_{control} > v_{tri}$	ON		OFF		E
$v_{control} < v_{tri}$	OFF		ON		-E

The inverter switching frequency is determined by the frequency of v_{tri}. The frequency ratio of v_{tri} to $v_{control}$ is known as the modulating frequency ratio m_f or simply $m_f = \frac{f_{tri}}{f_{control}}$. The amplitude modulation ratio m_a is the ratio of the peak amplitudes of $v_{control}$ to v_{tri} or simply $m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}}$.

3.5 Unipolar Sinusoidal PWM Control

Unipolar sinusoidal PWM control operates in the same way as the bipolar method with the exception that for each half cycle of $v_{control}$ the load voltage v_L is only of single polarity. This effectively halves the switching potential difference which results in reduced magnitudes of the output harmonics.

Switching of the transistors is done independently which results in four intervals per $v_{control}$ cycle as illustrated in table 3.2. For two intervals v_L equals E or –E which forces the load current to increase exponentially in the positive or negative direction respectively. This is similar to the bipolar method but the unipolar method differs for the remaining two intervals where the supply is isolated from the load. In these intervals the inductive load discharges through the remaining energised transistor and the opposite feedback diode. Figure 3.4 illustrates the voltages v_{AN}, v_{BN} and v_L with respect to $v_{control}$ and v_{tri}.

Table 3.2: Transistor Switching Strategy (Unipolar).

Transistor	T_{A+}	T_{B-}	T_{B+}	T_{A-}	v_{AN}	v_{BN}	$v_L = v_{AN} - v_{BN}$
$v_{control} > v_{tri}$	ON		OFF		E	0	E
$v_{control} < v_{tri}$	OFF		ON		0	E	-E
$-v_{control} > v_{tri}$	ON	OFF	ON	OFF	E	E	0
$-v_{control} < v_{tri}$	OFF	ON	OFF	ON	0	0	0

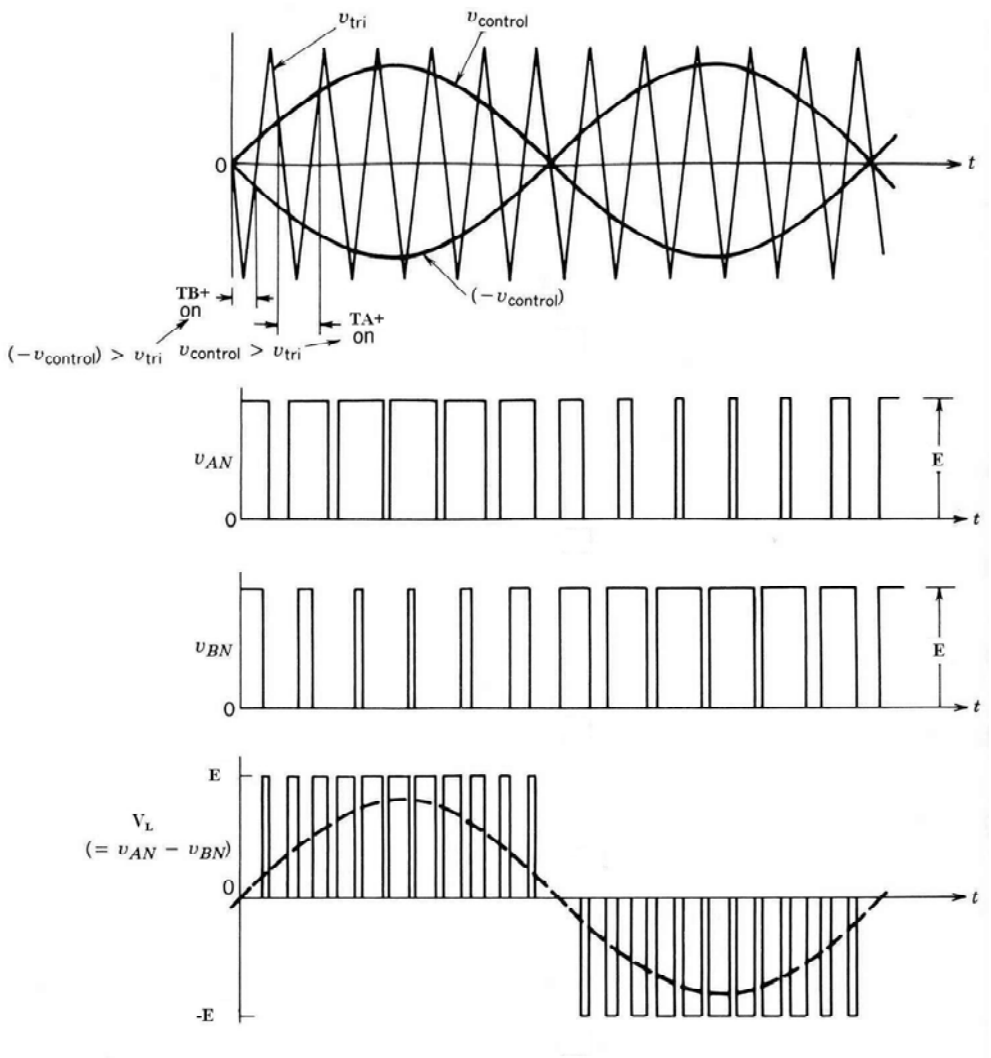


Figure 3.4: Unipolar Sinusoidal PWM Waveforms (Mohan et al. 1985).

3.6 Harmonic Content of the Unipolar Method

Comparisons of the harmonic content of the unipolar and bipolar sinusoidal PWM methods show that the unipolar method has the ability to produce less harmonics and at lower amplitudes than the bipolar method. The reason for the lower harmonic amplitudes is because the unipolar voltage switching difference of E is half the bipolar method of 2E, i.e. from E to –E.

The other advantage is derived from the fact that the unipolar method effectively doubles the switching frequency of the bipolar method. To take advantage of this, the frequency modulation ratio m_f should be chosen to be even. This results in the even harmonics having the same phase because the voltage waveforms of v_{AN} and v_{BN} are displaced by 180° of the fundamental frequency (Mohan et al. 1985). With the load voltage being the difference of v_{AN} and v_{BN}, the dominant harmonic component at the switching frequency in the output voltage v_L will cancel. In addition, the sidebands of the switching frequency harmonics will also cancel as will the dominant harmonic at twice the switching frequency. The outcome of this setup is that the unipolar method will only produce odd numbered harmonics.

If the amplitude modulation ratio is made less than one, the resulting equation for the harmonic order h can be written as the following (Mohan et al. 1985).

$$h = j\left(2m_f\right) \pm k \text{ for } m_a<1;$$

Where h = harmonic order

m_f = frequency modulation ratio

k = odd integer

m_a = amplitude modulation ratio

The photovoltaic system was designed to operate using the unipolar method over the bipolar method because of the advantage of reducing the inverter output harmonics. Although the bridge inverter load voltage will always be a square-wave, current control techniques provide regulation of the output current waveform. The following chapter provides an overview of common current control methods available and concludes with a detailed analysis of the tolerance band technique implemented by the photovoltaic system.

Chapter 4 CURRENT CONTROL TECHNIQUES

As previously discussed, the photovoltaic system utilises a square-wave inverter to connect the DC supplied by the photovoltaic cells to the AC power grid. Implementing a current-modulating technique will allow the inverter to produce a sinusoidal output and limit the DC content. Current control techniques are often used in power electronics applications to provide improved control, stability and speed of response. A popular example of this is the DC to AC motor drive where the AC motor speed and torque can be controlled by the inverter (Rashid 1988).

There exists many current-modulating techniques but all are designed with the same principle motive, to produce a specific inverter output waveform by controlling the duty cycle of the gate switching. Most techniques offer control of the inverter output at the current controller input. Many of these are open-loop and require either a predetermined modulating and carrier signal or a reference level and a fixed period of oscillation. These techniques have the ability to vary the output waveform but do not offer full feedback control. This was not desirable with the photovoltaic system because the inverter output would be required to match the grid at any instantaneous time and therefore a closed-loop technique was required that monitored the grid and controlled the inverter output accordingly. The tolerance band current control technique is a closed-loop current control technique that does not use a modulating signal or fixed period and was therefore implemented in the photovoltaic system.

This chapter starts by outlines the basic principles behind common modulation techniques and continues with an overview of the fixed frequency and constant off time current control techniques. The chapter concludes with a detailed analysis of the tolerance band current control technique.

4.1 Common Modulation Techniques

Many of the available current control techniques use modulation control. These operate with the same principles as the sinusoidal pulse-width modulation techniques described in the previous switch-mode inverter chapter. That is, they compare a carrier signal with a modulating signal to control switching of the inverter gates. A few of these techniques are the trapezoidal, staircase, stepped and harmonic injection modulation (Rashid 1988). All of these techniques use a triangular wave as the carrier signal and only differ by the waveform of the modulating signal. The name given to each of the modulating techniques often correspond to the shape of the modulating signal. For example: the trapezoidal, staircase and stepped techniques all have coinciding modulating signals.

One technique whose modulating waveform does not bear a resemblance to the shape of its name is the harmonic injected modulation technique. This is an advanced technique that generates a modulating signal by adding selected harmonics to a sinewave (Rashid 1988). This technique was designed to reduce the harmonic content in the output voltage by provide a higher fundamental amplitude (Rashid 1988). It also reduces the amount of over modulation resulting in less distortion of the output voltage. The modulating signal is commonly formed by the equation $v_m = 1.15\sin\omega t + 0.27\sin 3\omega t - 0.029\sin 9\omega t$. The typical shape of the modulating signal produces by this equation is illustrated in Figure 4.1. This figure demonstrates the harmonic injected modulation technique and includes an example of the inverter output with respect to comparison of the carrier to modulating signal for bipolar operation.

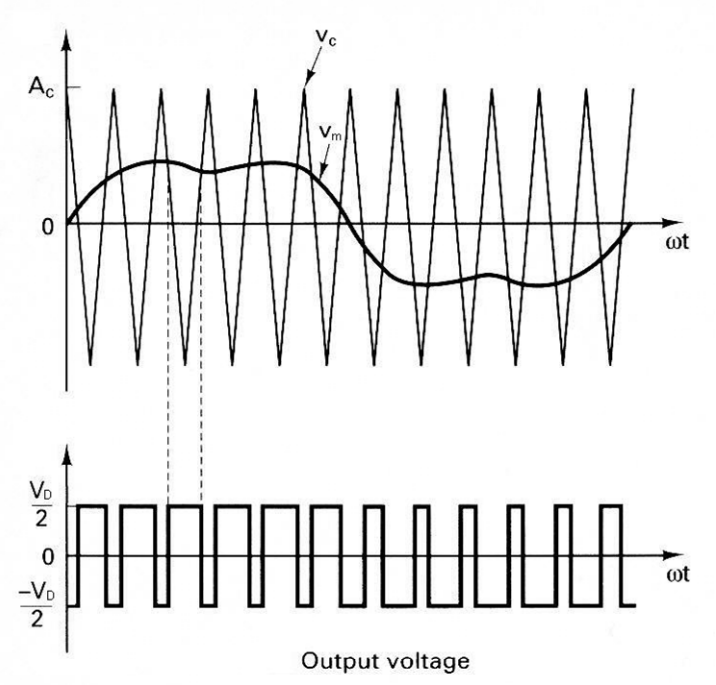


Figure 4.1: Harmonic Injection Modulation (Rashid 1988).

4.2 Fixed Frequency Current Control

To improve control of the inverter output current, closed-loop control techniques can be implemented that utilise negative feedback sourced from sensing the output current. There a various closed-loop current control methods, one of which is the fixed frequency current control technique.

Figure 4.2 shows a block diagram of the fixed frequency current control technique. It illustrates the use of a current sensor, summing junctions, a PI controller and a comparator circuit. Operation of the circuit starts by summing i_{ref} with i_{sen} to determine the error. The error is amplified or passed through a PI controller to give an output $v_{control}$, which is compared with a fixed frequency triangular or sawtooth waveform to determine the state the inverter switches.

There are only two possible outputs from the comparator, either logical high or low. With reference to a single-phase square-wave inverter this would usually control the state of the *A-side* switch. For example, if the error were below the reference current then the appropriate switch would remain energised so that the inverter output current would continue to rise. Once the error reaches the reference current then the appropriate switch is de-energised which results in a reducing inverter output current. The comparator remains in this state until the sawtooth waveform drops to zero with which the comparator resets, thus, re-energising the switch. Figure 4.3 illustrates a simplified version of this process. It clearly demonstrates that the switches controlling the inverter output current are reset after a fixed period, which is the period of the sawtooth frequency.

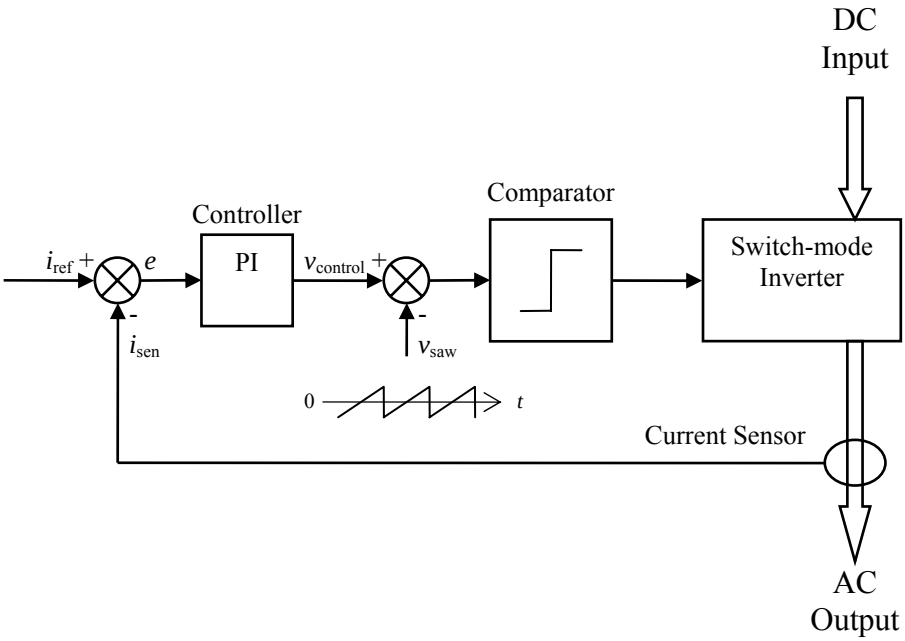


Figure 4.2: Fixed Frequency Current Control Block Diagram.

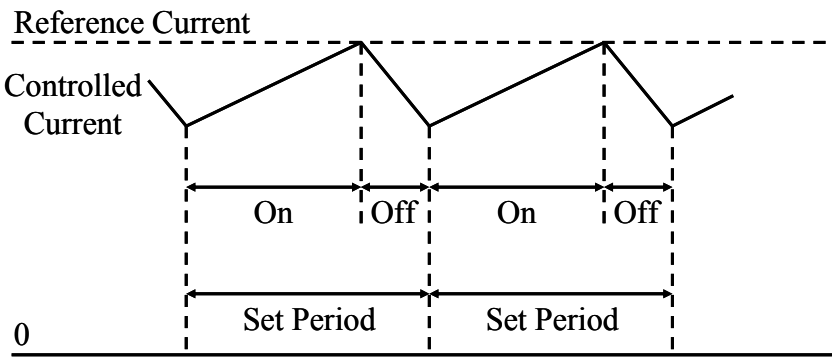


Figure 4.3: Fixed Frequency Current Control.

4.3 Constant Off Time Current Control

The constant off time current control technique operates in the same way as the fixed frequency technique with the exception that the sawtooth waveform is only introduced once the error reaches the reference current. This results in the appropriate switch remaining off for a fixed period. Therefore the on time for the energised which is not fixed and remains on until the error reaches the reference current. Figure 4.4 illustrates this process.

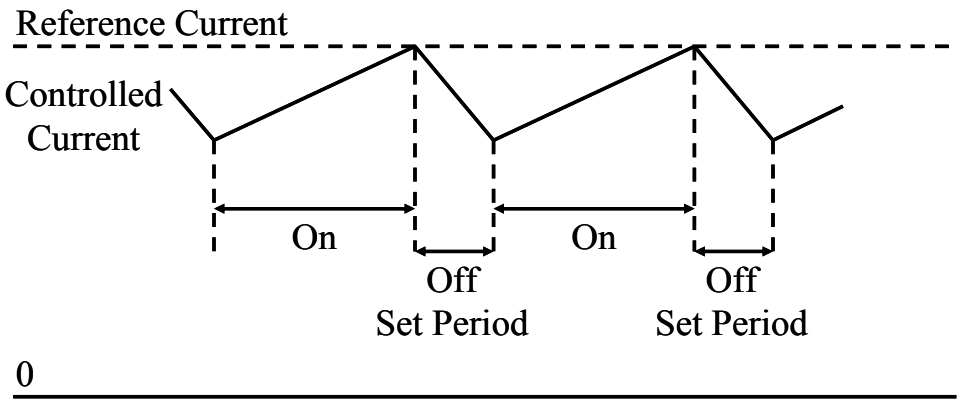


Figure 4.4: Constant Off Time Current Control.

4.4 Tolerance Band Current Control

The tolerance band current control technique, also referred to as hysteresis or delta modulation (Rashid 1988), is a closed-loop technique that controls both the on and off time of the inverter switches without using a fixed period. This is achieved by implementing a comparator and latch circuit and therefore no sawtooth waveform is required. A block diagram of the tolerance band current control method is displayed in figure 4.5.

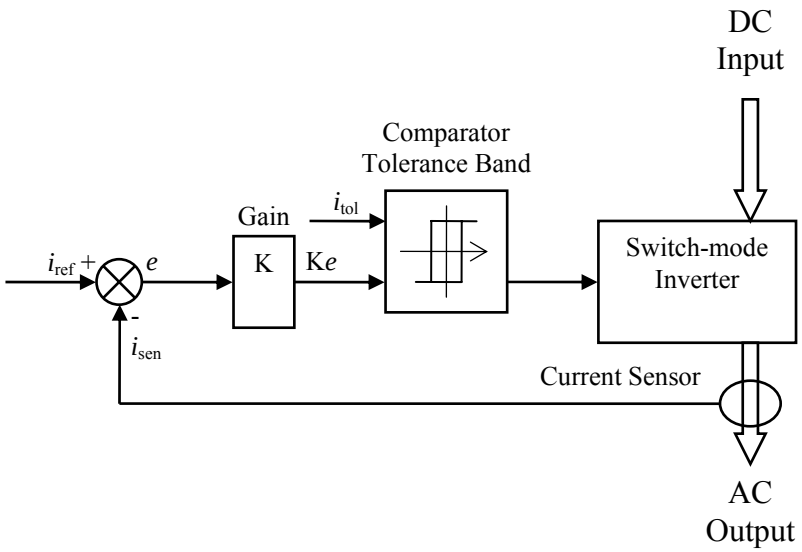


Figure 4.5: Tolerance Band Current Control Block Diagram.

Operation of the circuit begins by summing the reference and sense current, with the resulting difference being the error. The error is amplified and then compared to the tolerance band. If the error lies between the upper and lower tolerance band then no change takes place in the comparator latch circuit. Once the error reaches either the upper or lower tolerance band the output is changed and remains in that state until the error reaches the opposite tolerance band. Figure 4.6 illustrates this process.

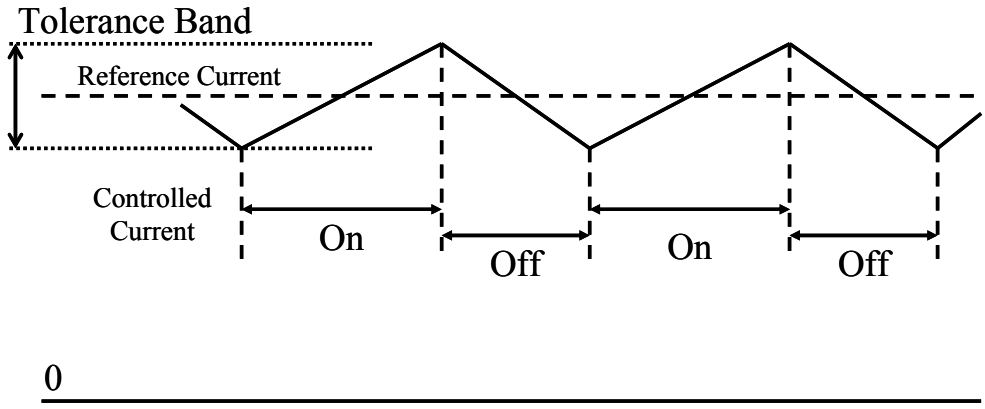


Figure 4.6: Tolerance Band Current Control.

With reference to the single-phase square-wave bridge inverter used in the photovoltaic system, unipolar operation of the tolerance band technique is as follows. Starting with positive polarity and opposite transistors *TA*+ and *TB*- are both on. The inverter output current rises until it reaches the upper tolerance band with which the *T*A+ transistor is turned off and the current is forced to flow through the feedback diode DA-. This results in the output current decreasing until it reaches the lower tolerance band, when at this instance transistor *A*+ is re-energised. The process is repeated until the reference current reverses polarity and the both the *TA*+ and *TB*- transistors are de-energised. The system is now operating with negative polarity and therefore the switching transistor are *TA*- and *TB*+. The tolerance band current control process is repeated with transistor *TA*- being the controlled switch. Figure 4.7 illustrates this by showing the energised transistors during one cycle of inverter output using unipolar operation.

Adjusting the magnitude of the tolerance band varies the duty cycle of the transistor switching. This has the effect of controlling the ripple content of the output waveform. Therefore, to achieve an output waveform with minimum ripple content, the magnitude of the tolerance band must be reduced. Due to the finite switching time taken for all non-ideal electronic components, the ripple content cannot be reduced to zero. There will always be a limit where saturation will occur. Common PWM techniques switch the transistors at approximately 100 times the inverter output frequency.

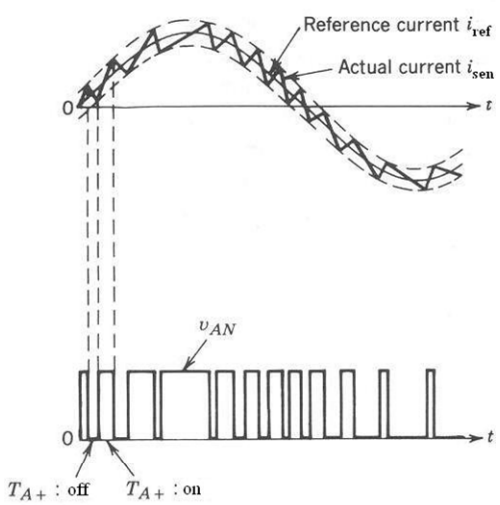


Figure 4.7: Tolerance Band Waveform and Inverter Switching (Mohan et al. 1985).

Chapter 5 CURRENT CONTROLLER IMPLEMENTATION

With the fundamental components of the current controller system covered, it is now necessary to understand operation of the existing current controller circuit and how to integrate it into the photovoltaic system.

As stated in chapter 2, the current controller system requires additional gate drivers and optocouplers. This is because the output signal from the current controller circuit cannot provide enough current to ensure successful turn-on of the inverter transistors. Gate drive circuits are high speed switching circuits that provide this power. Optocouplers are used to provide electrical isolation between the inverter and current controller so that each can have an independent voltage reference.

The chapter starts with a description of the principle operation of the current controller and provides a simplified operational diagram of the current controller circuit. It continues with an overview of a typical gate drive circuit and provides a detailed analysis of the gate driver used during testing. The chapter concludes by outlining the need for independent voltage references and provides details of the optocouplers used during testing.

5.1 Current Controller Circuit Operation

This section is provided to explain the principle operation of the current controller. The complete electrical schematic is displayed in appendix B, while figure 5.1 provides a simplified operational diagram of the circuit.

The current controller circuit begins with a zero crossing input to determine polarity of the reference signal and hence, allow operation of either transistors (*TA*+ and *TB*-) or (*TA*- and *TB*+). The 5k variable resistor across pins 5 and 6 of the LM311 voltage comparator provides tuning of the zero volt crossing. This should be set before operating the current controller by grounding the V_z input and tuning to give zero volts output of the comparator. This leg of the current controller circuit provides a direct gate output for the *B-side* transistors and allows operation of the *A-side* transistors in the current control latch circuit. Operational transistors for the positive and negative reference current cycles are (*TA*- and *TB*+) and (*TA*+ and *TB*-) respectively. There is a series RC circuit to provide a small time delay during transistor changeover to prevent shorting the inverter supply rails.

The current control circuit begins by summing the negative feedback sensed at the inverter output and the reference signal to give a total error. This error is then amplified by passing through a gain circuit. The amplified gain, K*e*, is then compared to the tolerance band input which controls the set and reset of a latch circuit. The latch circuit controls the *A-side* transistors. The tolerance band input is controlled externally and needs to be set to the desired level of tolerance. This controls the ripple content of the inverter output current and therefore, by reducing the tolerance band input, the ripple content decreases resulting in a smoother output waveform. This increases the transistor switching frequency and because of time delays in the switching of real components there is a limit to how fast the transistors can be switched before saturation occurs.

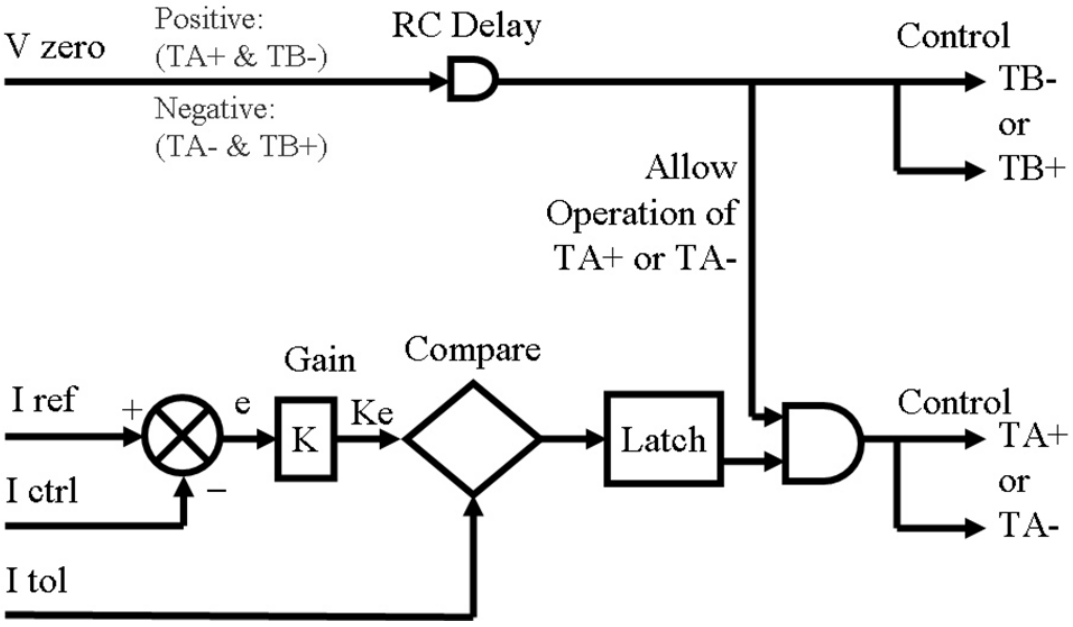


Figure 5.1: Current Controller Circuit Operation.

5.2 Gate Drive Circuit

The output of the current controller provides the switching signal for the inverter transistors. This signal is sourced by CMOS schmitt triggers contained in the MC140106 chip but is inadequate in providing the required voltage and current levels to successfully control the transistors. For this reason a gate drive circuit is required to amplify the logic signal from the current controller output. Gate drive circuits can be constructed using standard electronic components as illustrated in figure 5.4. This particular circuit illustrates the use of an optocoupler to isolate the signal source and is only designed to provide the gate current for a single IGBT. The design of these circuits can be quite demanding and the challenge is made even more difficult when requiring both a high and low side driver. This was the case for the inverter used in the current controller system and therefore an easier and more cost effective way was to use a gate driver that contained all the complex circuitry in a single chip.

The gate driver used in the testing phase of the current controller system was the IR2113 high and low side driver by International Rectifier. The pinout diagram and pin description are displayed in figure 5.5 and table 5.1 respectively.

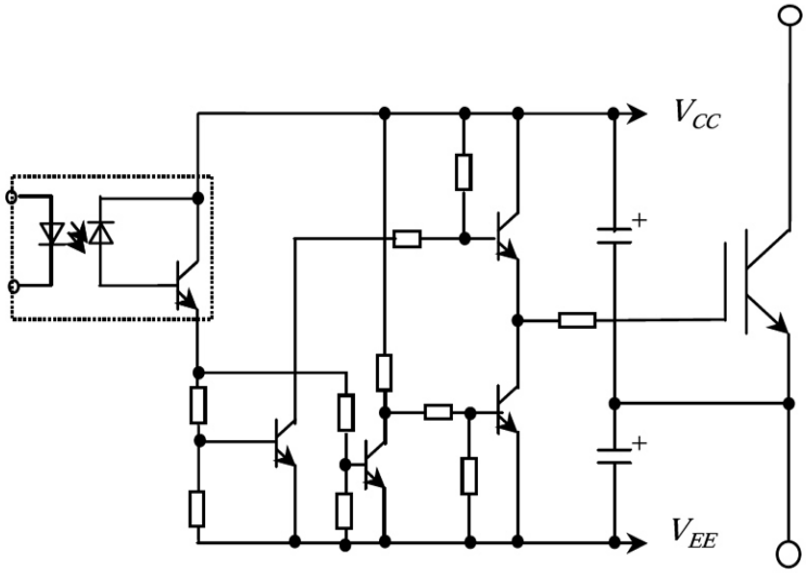


Figure 5.2: Single Gate Drive Circuit (Fuji Electric 2005).

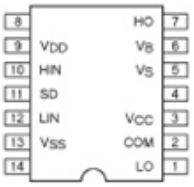


Figure 5.3: IR2113 Pinout Diagram (International Rectifier IR2113).

Table 5.1: IR2113 Pin Description (International Rectifier IR2113).

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Figure 5.6 illustrates the functional block diagram of the internal circuitry of the IR2113 gate driver. It illustrates independent high and low side output channels. This allows an independent voltage level shift for the high side transistor. The device is designed to drive n-channel IGBTs up to 600V (International IR Rectifier IR2113). The logic inputs are both CMOS and TTL compatible. The driver is not a stand alone device and requires external connection of a bootstrap diode and capacitors as illustrated in figure 5.7. The bootstrap diode is required to operate at high speed and be capable of handling high bursts of current flow, typically in the tens of amps. The part used during testing was a PBYR1645 Fast Schottky Diode by Phillips.

The bootstrap capacitors provide the current source for the transistor gates. The basic principle of operation is to have one bootstrap capacitor discharge into the transistor gate while the opposite capacitor charges. The supply to these capacitors is provided by V_{CC} and the bootstrap diode prevents the high side capacitor from discharging into the low side capacitor. This cycle is repeated at the rate of the transistor switching frequency.

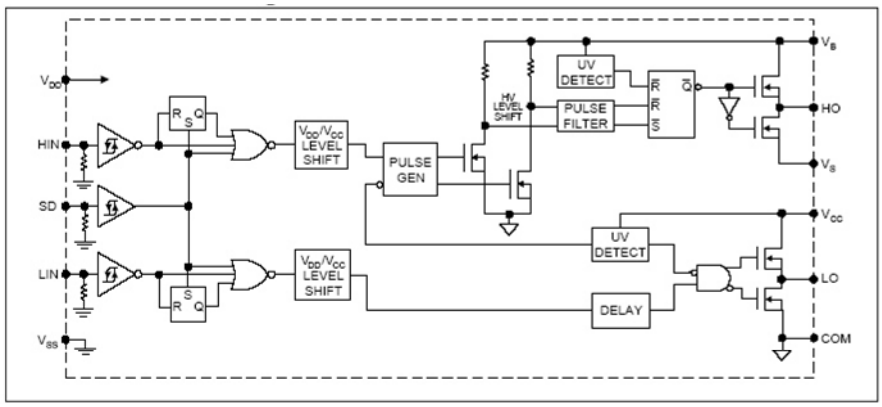


Figure 5.4: IR2113 Functional Block Diagram (International Rectifier IR2113).

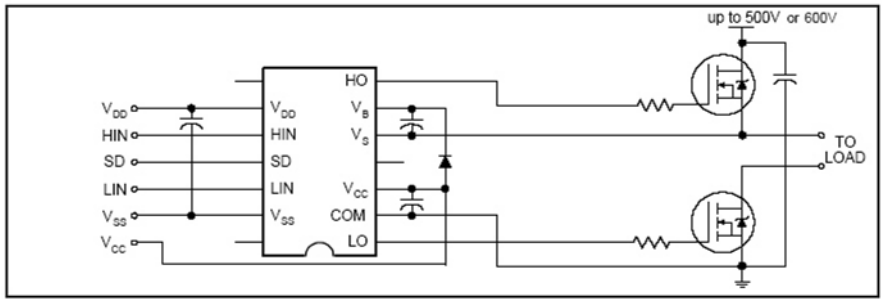


Figure 5.5: IR2113 Typical Connection (International Rectifier IR2113)

5.3 Optocouplers

Another issue faced with controlling the inverter transistors is that the reference voltage cannot be the same for both the high and low side transistors. This is because the emitter of the high side transistor is directly connected to the collector of the low side transistor and therefore both emitters cannot have the same voltage reference. This causes the problem of not being able to simply supply the high side transistor gate with the same signal as the low side. The gate drive circuit overcomes this problem by providing a voltage level shift to the high side transistor base and therefore equalising the base-emitter voltage for both transistors. This is usually done in conjunction with electrically isolating the inverter circuit with the control circuit so that ground references can be independent of each other. There are a few methods commonly used to achieve this isolation, one of which is to interface optocouplers between the controller and inverter. The current controller system uses this method by passing the output of the current controller through optocouplers before feeding the logic inputs of the gate drive circuit.

The specific component used during testing was the Fairchild Semiconductor HCPL-2503 optocoupler. The pinout diagram is shown in figure 5.2. This figure also illustrates the internal components of the IC which consists of an LED optically coupled to a transistor. The transistor is a high-speed photo-detector that permits logical switching up to 1 Mbps, permits insulation protection up to 480 V and is compatible with both CMOS and TTL technology (Fairchild Semiconductor HCPL-2503).

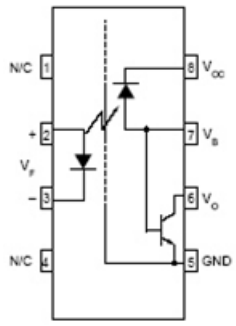


Figure 5.6: HCPL-2503 Pinout Diagram (Fairchild Semiconductor HCPL-2503).

An important electrical characteristic that had to be considered while incorporating a transistor controlled optocoupler in the current controller system was the propagation rise and fall times. This was due to the high speed switching generated by the pulse width modulation control technique and the requirement to have reactions times in the low microseconds when the error reached the tolerance band. Figure 5.3 displays a plot sourced from the HCPL-2503 data sheets of the typical propagation delay times with respect to temperature. It demonstrates a maximum delay time at 25° of approximately 530 and 420 ns for low-high and high-low transitions respectively. This time was less than the acceptable time of approximately 1μs and therefore guarantied successful implementation into the photovoltaic system

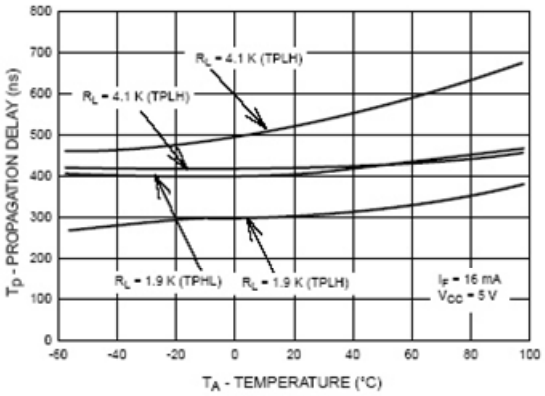


Figure 5.7: HCPL-2503 Propagation Delay (Fairchild Semiconductor HCPL-2503).

Chapter 6 SYSTEM ANALYSIS AND TESTING

To prove correct operation of the current controller, a temporary circuit including the gate drive and switch-mode inverter was constructed. Initial testing was conducted in open-loop by proving sections of the complete circuit for correctness and then closing the circuit with negative feedback to produce the final sinusoidal output. Once the circuit was proven a printed circuit board of the current controller was designed and constructed. An image of the PCB is displayed in appendix B.

The following sections of this chapter provide details of the components used, tests conducted and results obtained for each section of the current controller system.

6.1 Components List for Current Controller System Testing

Table 6.1 provides a list of the main components used to construct and test the current controller system. This table is provided as a guide for future work but equivalent parts may be substituted.

Table 6.1: Components List for Current Controller System Testing.

Current Controller			
Part	Description	Manufacturer	Quantity
LM308	Operational Amplifier.	National Semiconductor	4
LM311	Voltage Comparator.	National Semiconductor	3
CD40106	CMOS Hex Schmitt Triggers.	Texas Instrument	1
MC14044	Quad-NAND RS Latch	Motorola	1
MC14071	Quad 2-Input OR Gate.	Motorola	1
MC14081	Quad 2-Input AND Gate.	Motorola	1
Resistors	5k Trim Pot		1
	1.5k		1
	3.3k		1
	4.7k		2
	8.2k		1
	15k		5
	27k		2
	56k		2
Capacitors	33p		4
	100p		1
	330p		2
	10n		1
Optocouplers			
HCPL-2503	High speed transistor optocoupler (Single channel).	Fairchild Semiconductor	4
Gate Drivers			
IR2113	High and low side gate driver.	International Rectifier	2
PBYR1645	Fast Schottky Diode	Philips	1
Bridge Inverter			
IRG4BC30KD	IGBT with ultra fast soft recovery diode.	International Rectifier	4

6.2 Zero Crossing Section

The first section tested was the zero crossing circuit. Its primary function is to control the output for the IGBT gate drive circuit. There are only two situations possible. The first is when the input voltage V_Z is positive and the second when it is negative. For the first situation, gate *B*- is energised and *A*+ is made functional. For the second situation, gate *B*+ is energised and *A*- is made functional.

Before supplying the circuit with V_Z the 311 comparator output needed to be tuned to give zero volts output for zero volt input. This was to ensure that switching was done as close to zero as possible for the oscillating input signal. Tuning was achieved by grounding the positive input pin 2 and then adjusting the trim pot until the output was zero. The next step involved replacing the ground to pin 2 with a 6 Volt 50 Hz signal. The supply came from a 12 VAC source with a 10 kΩ pot used to lower the input voltage. The complete circuit is illustrated in figure 6.1 below.

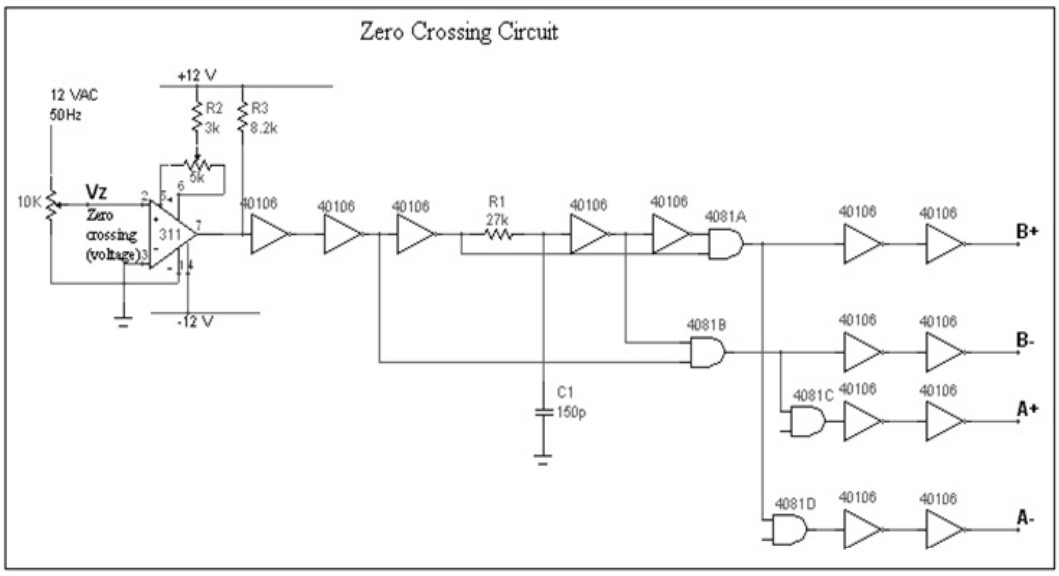


Figure 6.1: Electrical schematic of zero crossing circuit.

Testing proved that the logic output from the comparator changed from high to low as V_Z changes from positive to negative. Correct logic was also confirmed through the inverters to the gate outputs. The next important process to confirm was the delay between changing gate outputs to prevent IGBT's momentarily shorting at changeover. The time delay was achieved with a simple R-C circuit which delayed the high level input to a 2-input AND gate. Figure 6.2 illustrates a delay of approximately 7 μs between the inverter output going high and the AND gate output going high to turn gate *B*+ on. Figure 6.3 illustrates the resulting delay between gate *B*- turning off and gate *B*+ turning on.

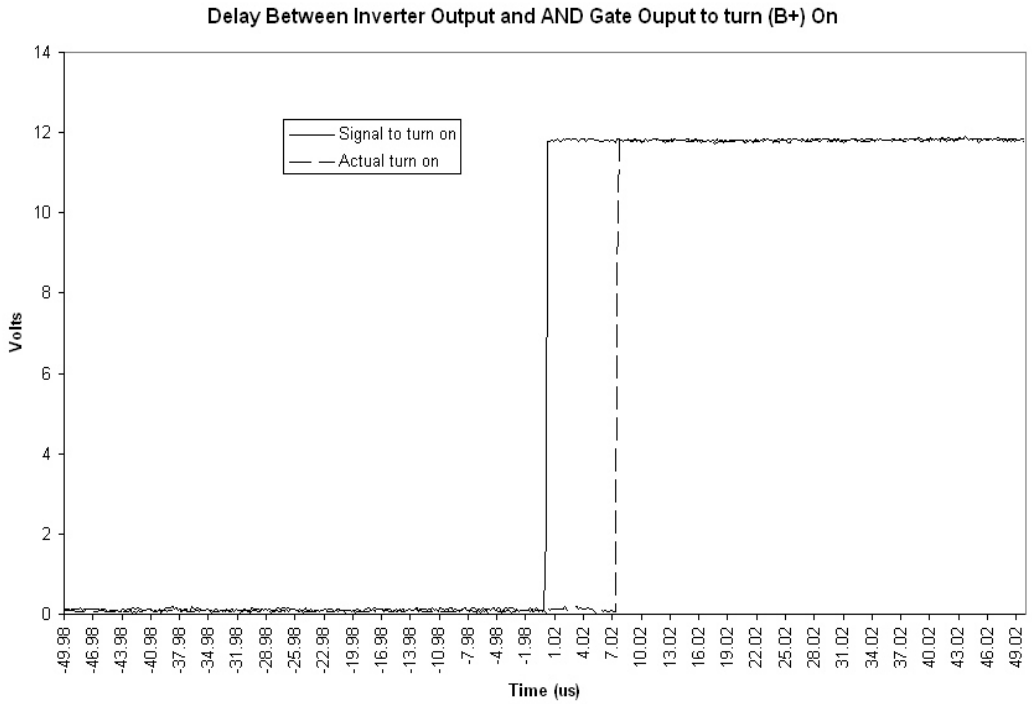


Figure 6.2: Oscilloscope image demonstrating delay to turn gate *B*+ on.

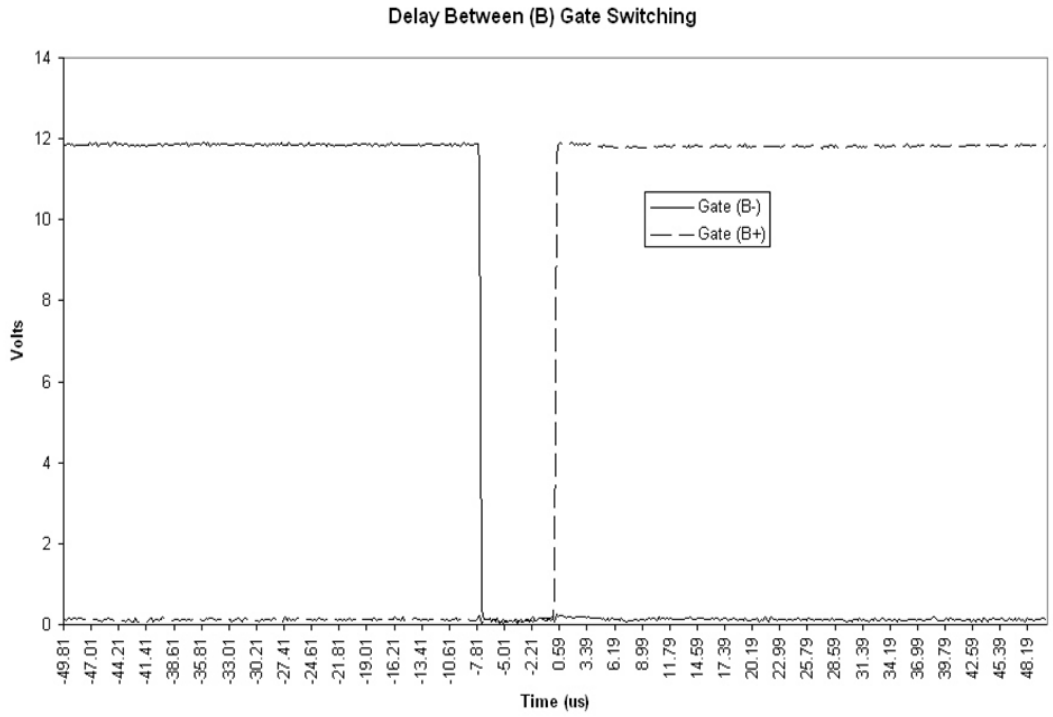


Figure 6.3: Oscilloscope image demonstrating delay between gate switching.

6.3 Error and Latch Circuit

Testing of the error and latch circuit began by supplying the $i_{sen,}$ i_{ref} and I_{tol} inputs with -2, +1 and +2 volts respectively. This was achieved using a 12 volt source and adjusting 10 kΩ pots to produce the desired output voltage. Figure 6.4 illustrates this set up.

The next step was to check that the measured voltages at the summing and multiplying nodes were correct. A summary of the calculated and measured values at these nodes are given in table 6.1.

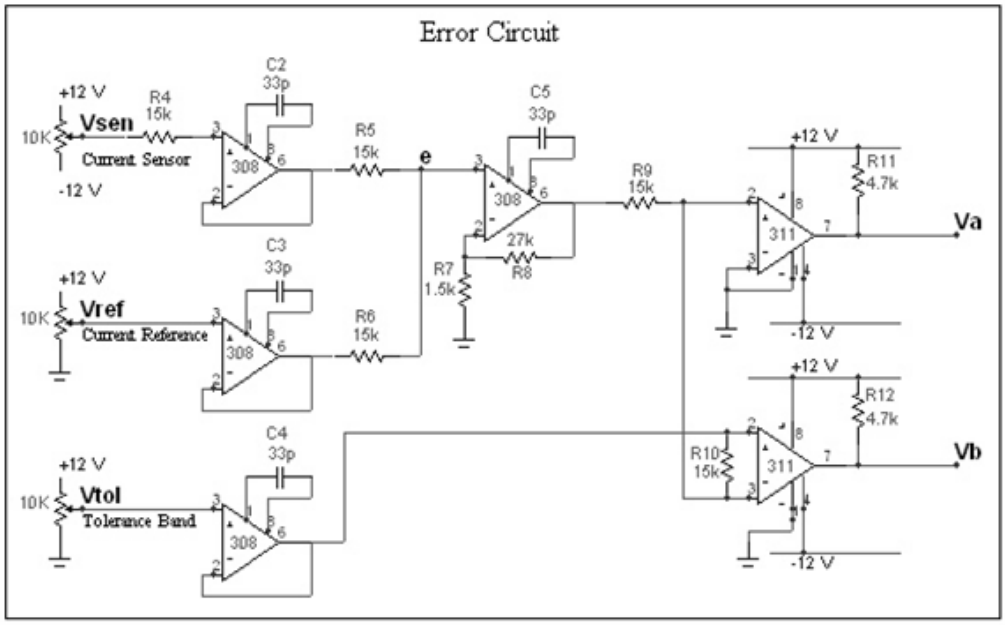


Figure 6.4: Electrical schematic of error circuit.

Table 6.2: Calculated and measured error values.

Node		e	Gain (K)	*Ke*	Summation at *Ke* and V_{tol}
General equation		$\frac{V_{sen}+V_{ref}}{2}$	$1+\frac{27}{1.5}=19$	$19\times e$	$\frac{Ke+V_{tol}}{2}$
Values for V_{sen} = -2 V V_{ref} = 1 V V_{tol} = 2 V	Calculated	-0.50 V	19	-9.50 V	-3.75 V
	Measured	-0.48 V	20	-9.60 V	-3.70 V

With the error circuit operating correctly the procedure to prove the latch circuit was to adjust the V_{sen} voltage and determine the correct logic outputs of the 311 comparators, labelled *Va* and *Vb* in figure 6.4. These outputs *Va* and *Vb* operate the latch IC set and reset inputs respectively. Once the 311 outputs were proven to be operating correctly the output logic of the 4044 IC was monitored which confirmed that the latch circuit was also operating correctly.

Table 6.2 illustrates the logic parameters for *Va* and *Vb* along with the truth table for the 4044 latch IC. The table also illustrates the calculated and measured voltages of error required to set and reset the latch. Figure 6.5 illustrates the electrical schematic of the latch circuit. The two 'noise delay' R-C circuits connecting the latch output to its input are for the purpose of providing a very short delay at the latch set and reset change over. This measure ensures smooth transitions by preventing unwanted oscillations due to CMOS sensitivity.

The final check proved that gate outputs *A*+ and *A*- were enabled when *Vz* was positive and negative respectively and that the latch circuit isolated the A gates according to the truth table. Figure 6.6 illustrates the *A* gate switching according to the polarity of V_Z and the comparison of error to tolerance.

Table 6.3: Logic parameters for latch circuit.

<table>
<tr><td>Output</td><td>Va</td><td>Vb</td><td>4044 latch IC</td><td colspan="2">V_Z</td></tr>
<tr><td>General Equation</td><td>Low when
$\frac{Ke+V_{tol}}{2}<0$
$\therefore Ke<-V_{tol}$</td><td>Low when
$V_{tol}<\frac{Ke+V_{tol}}{2}$
$\therefore V_{tol}<Ke$</td><td rowspan="3">Va controls set input.

Vb controls reset input.</td><td>Positive</td><td>Negative</td></tr>
<tr><td>Values of V_{sen} to change logic state when
V_{ref} = 1 V
V_{tol} = 2 V</td><td>-1.21 V</td><td>-0.79 V</td><td colspan="2">Enabled Gate</td></tr>
<tr><td></td><td></td><td></td><td>A+</td><td>A-</td></tr>
<tr><td>V_{sen} < -1.21</td><td>L</td><td>H</td><td>L</td><td>A+ On</td><td>A- Off</td></tr>
<tr><td>-1.21 < V_{sen} < -0.79</td><td>H</td><td>H</td><td colspan="3">Stay in same state</td></tr>
<tr><td>-0.79 < V_{sen}</td><td>H</td><td>L</td><td>H</td><td>A+ Off</td><td>A- On</td></tr>
</table>

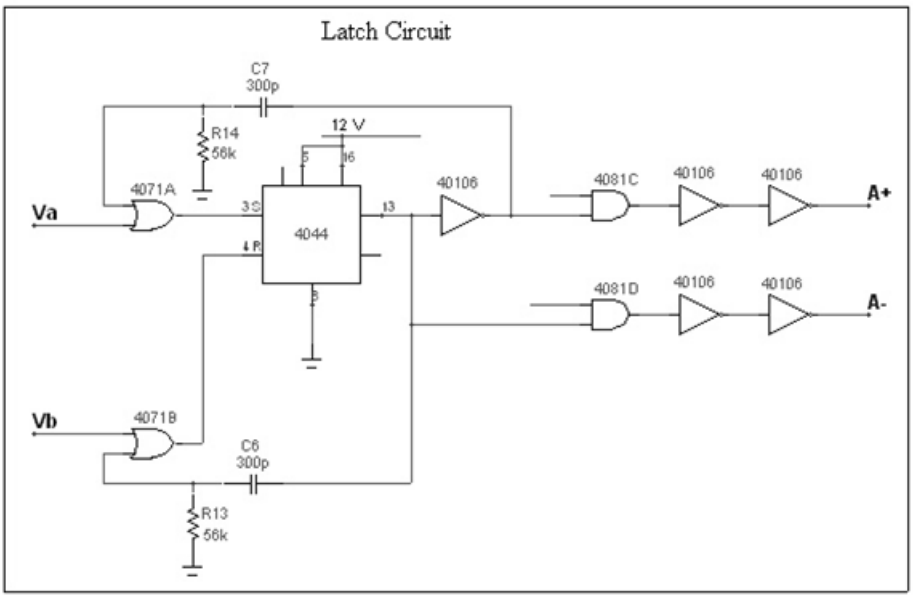


Figure 6.5: Electrical schematic of latch circuit.

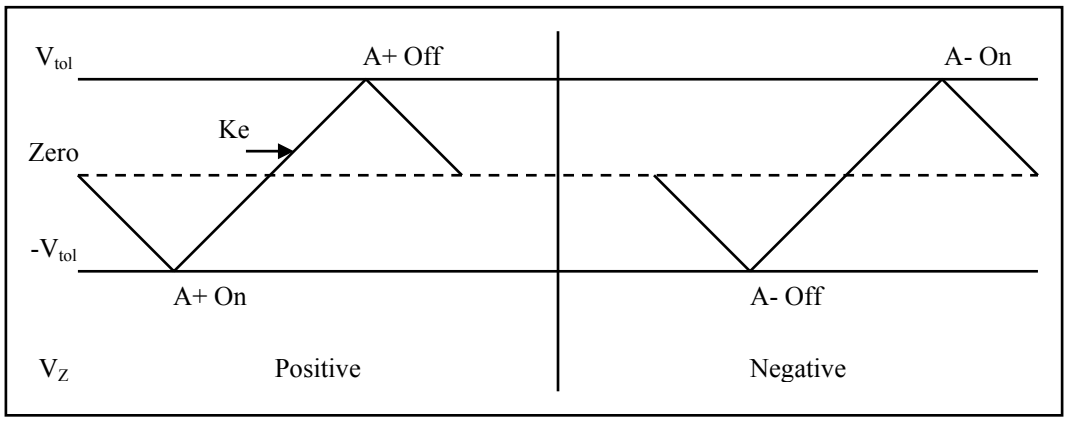


Figure 6.6: Illustration of *A* gate switching.

6.4 Gate Drive and Switch-mode Inverter Circuit

The next phase of testing was the gate drive circuit. A single IR2113 high and low side driver was used to supply the IGBT gates with enough current to ensure correct turn on. Care had to be taken with the selection of the bootstrap diode because it had to handle fast switching as well as a considerable amount of current. A PBYR1645 fast recovery schottky diode was used in the temporary test circuit and proved to be suitable. 2×IRGBC30KD IGBTs with internal soft recovery diodes were used to construct a temporary switch-mode inverter. The initial test used only a 10 kΩ resistive load as illustrated in figure 6.7. This would provide a square-wave output used to determine correct operation of the complete gate drive circuit. The gate drive inputs were controlled by the current controller B gate outputs. This provided a 50 Hz oscillation between + and – gates without interruption from the latch circuit. A 22 Ω resistor was placed in series with the IGBT's to prevent damaging the transistors in the event that they were energised simultaneously.

Figure 6.8 illustrates the gate drive high and low output voltages with respect to ground while figure 6.9 illustrates the square-wave output with respect to the sine wave input V_Z of the current controller. The purpose of figure 6.8 is to demonstrate the gate signal to transistor *A*+ turning off before *A*- is energised. Note that the emitter for transistor *A*+ is connected at the 15 V node and therefore the gate is off in the region where figure 6.8 demonstrates 15 V or less. The noise in transistor *A*+ turning off was varying throughout the testing procedure and it was concluded that it was generated by the inconsistency of the connections in the breadboard test circuit. This problem was not expected to occur in the final printed circuit board.

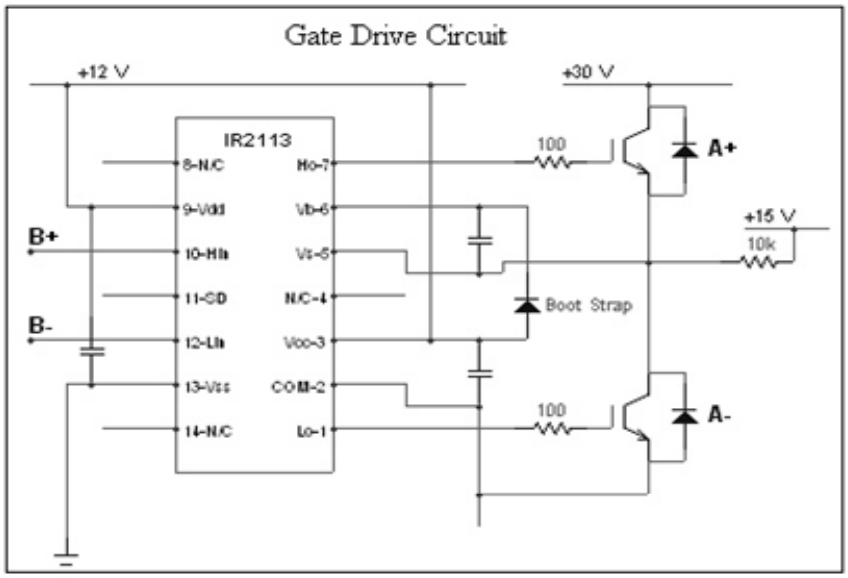


Figure 6.7: Electrical schematic of gate drive circuit.

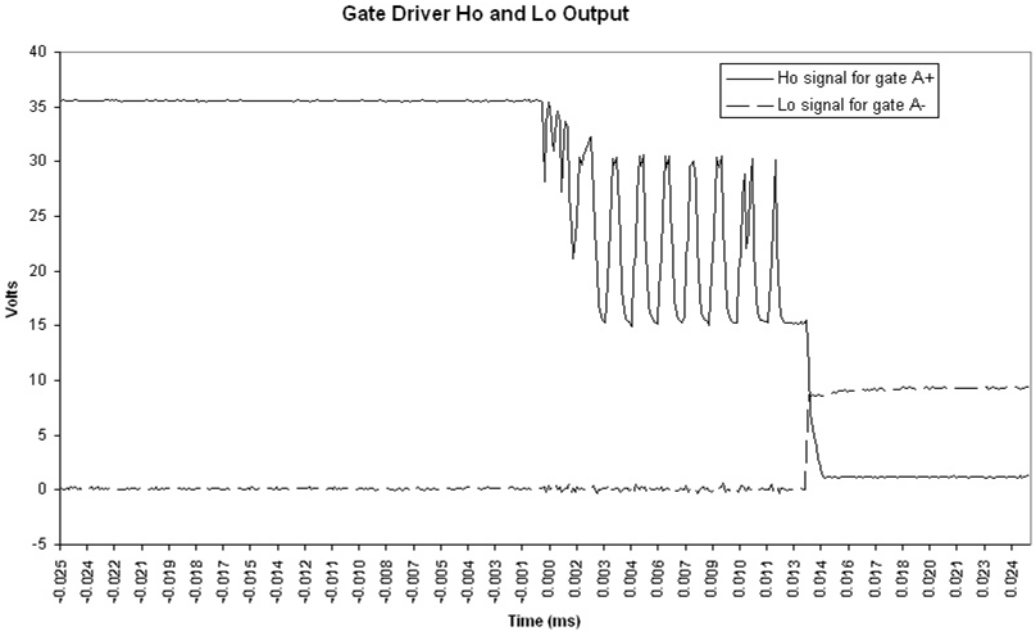


Figure 6.8: Oscilloscope image demonstrating gate driver Ho and Lo output.

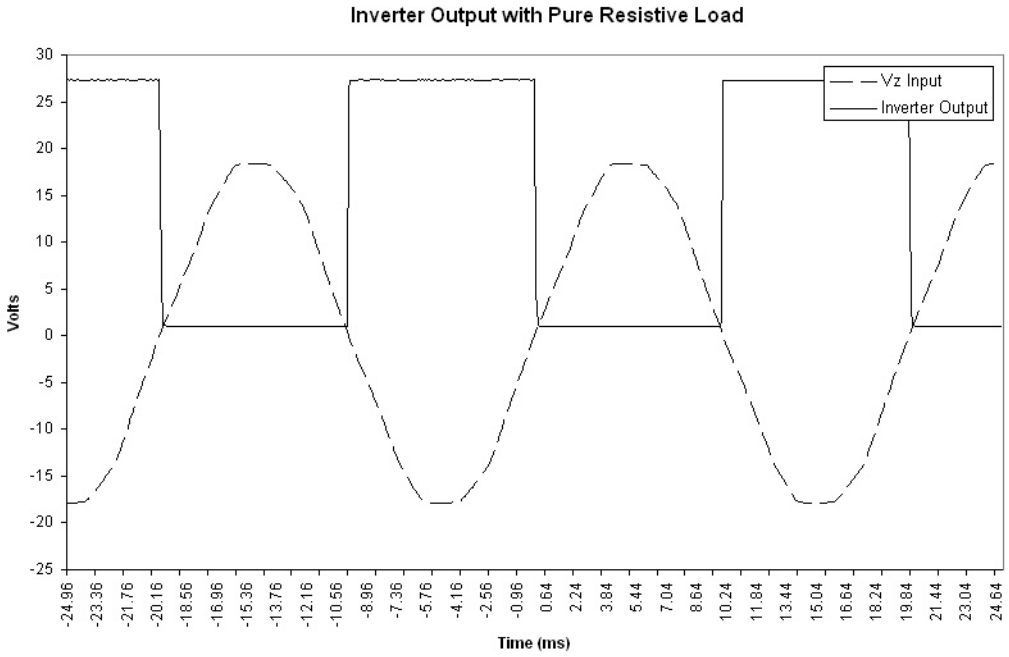


Figure 6.9: Oscilloscope image demonstrating inverter output with pure resistive load.

To generate an exponential output the 10 kΩ resistor was replaced with a 4.7 kΩ resistor and 1 μF capacitor circuit. The results are shown in figure 6.10 which demonstrate an exponential rise and fall of capacitor voltage with comparison to the oscillating high to low gate signal to transistor *A*+.

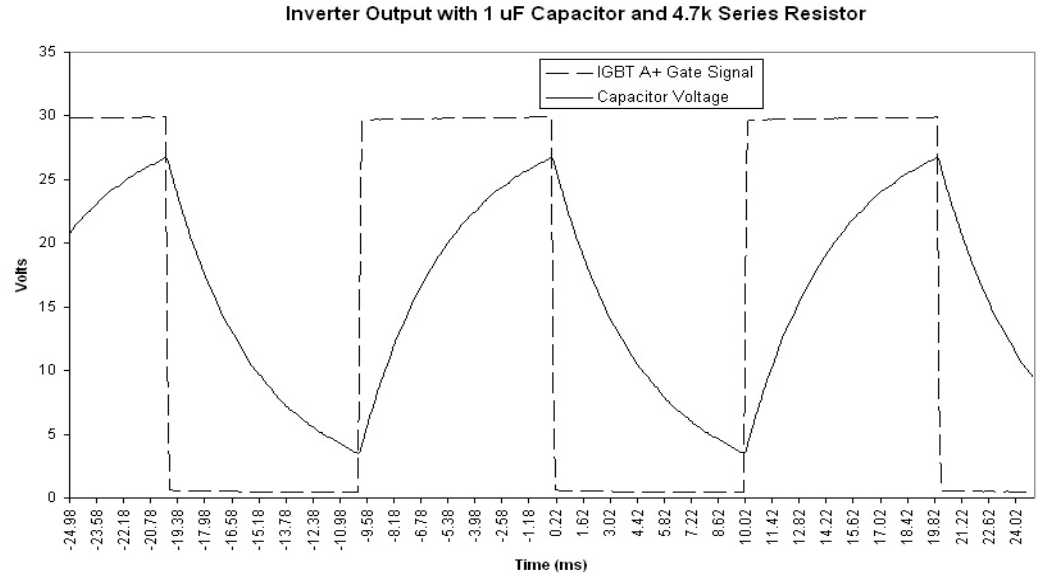


Figure 6.10: Oscilloscope image demonstrating inverter output with R-C circuit.

The inverter output oscillates about +15 V but the current controller required oscillation around 0 V. For this reason a differential amplifier circuit was constructed as illustrated in figure 6.11. Figure 6.12 illustrates the inverted output that would be suitable to provide a signal to the current sensor input of the current controller.

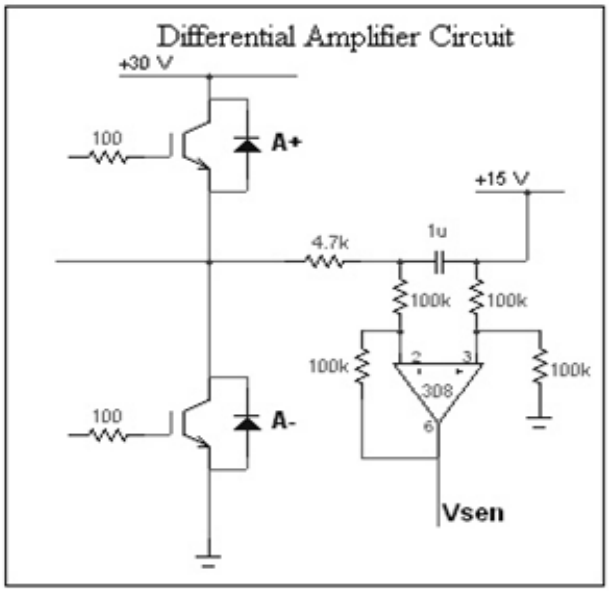


Figure 6.11: Electrical schematic of inverter with differential amplifier.

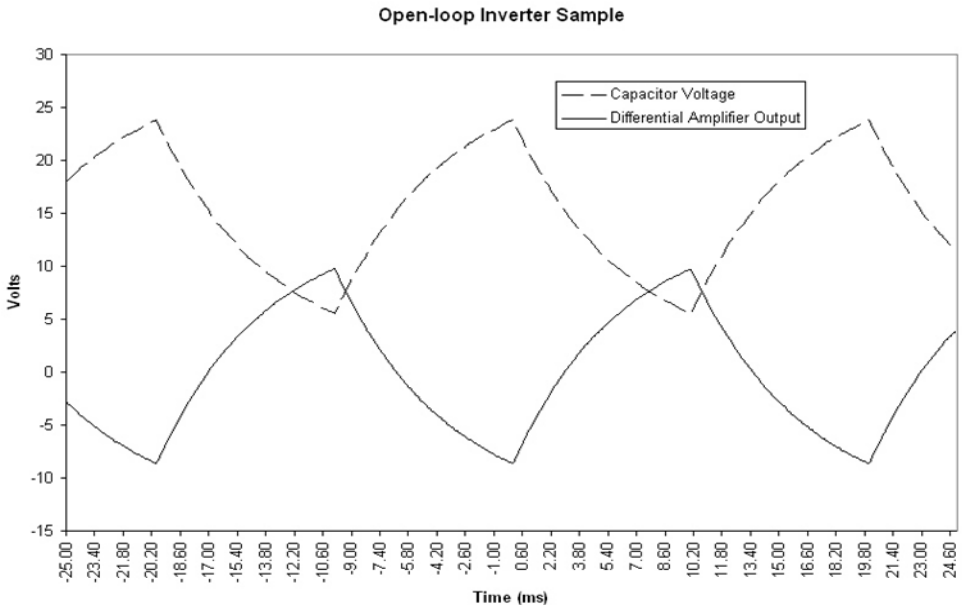


Figure 6.12: Oscilloscope image demonstrating differential amplifier output.

6.5 Closed-loop Tests and Results

With all open-loop tests functioning correctly the last test was to close the loop and analyse the entire circuit. To connect the circuit in closed-loop the current controller gate outputs, *A* and *B*, were connected to the corresponding gate drive inputs. The 2 VDC reference input to the current controller was replaced with a 5 volt peak ac signal via a 10 kΩ pot in parallel with the 12 VAC V_Z supply. This ensured that the reference voltage was in phase with the zero crossing voltage. The 10 kΩ pot connected to the current sensing input was removed with the new input connected directly to the inverter differential amplifier output. The last important change was to modify the inverter R-C network to function in unipolar mode because the open-loop was simulated by a bipolar method which allowed the capacitor to discharge through the *A*- transistor only for half of each cycle. In the closed-loop unipolar system the capacitor would be required to discharge many times for each half cycle without the use of the opposite IGBT. To perform this task the 4.7 kΩ series resistor was replaced with a 1 kΩ resistor and another 1 kΩ resistor was connected in parallel with the capacitor, this would be used as a charge/discharge path for the negative and positive half cycles respectively. The reduction in resistor values was used to shorten the R-C time constant to make the inverter more responsive. Care was taken not to make the time constant too short because as the rise and fall times become too steep the system would operate erratically.

Figure 6.13 illustrates the inverter output, or current sensor input, with the tolerance band set at 2 V. The plot also shows the switching of the *A*- and *A*+ transistors in the positive and negative half cycles respectively. It can be seen that the switching frequency was approximately 50 times the output sinusoidal frequency. By reducing the tolerance the switching frequency would be increased and a smoother output sine wave would result. Figure 6.14 illustrates this and compares the current sensor to the current reference at a tolerance of 0.16 V. Saturation started to occurred for values of $V_{tol} < 0.16$ V. The current sensor voltage is the inverse of the reference voltage because the controller uses a negative feedback to operate.

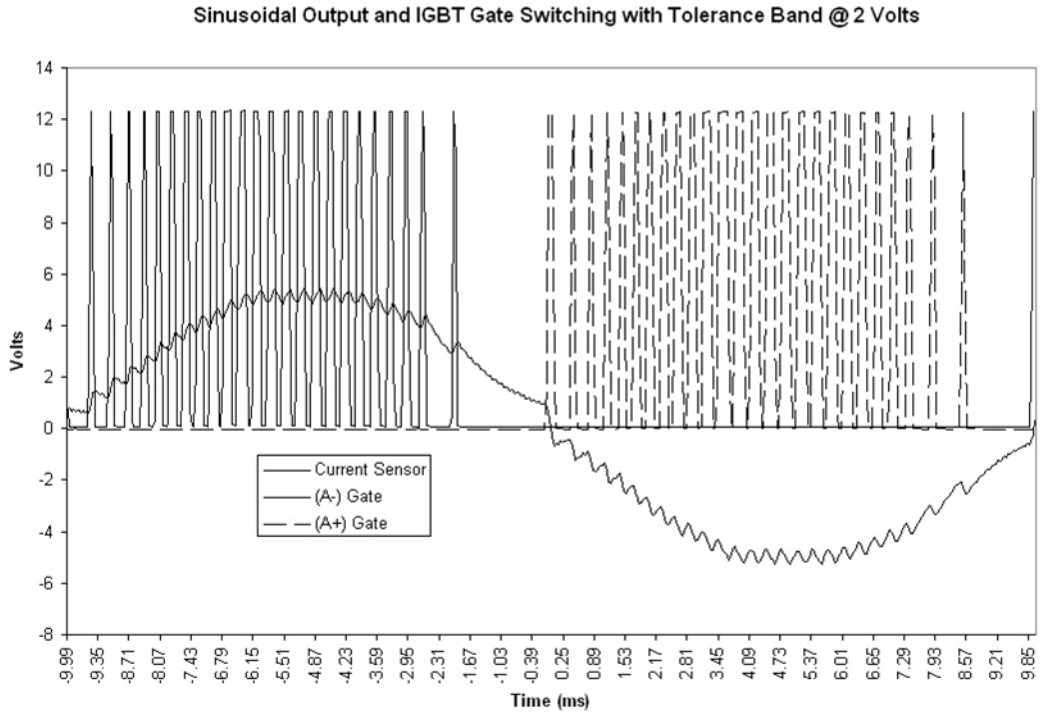


Figure 6.13: Oscilloscope image demonstrating sinusoidal output with IGBT switching.

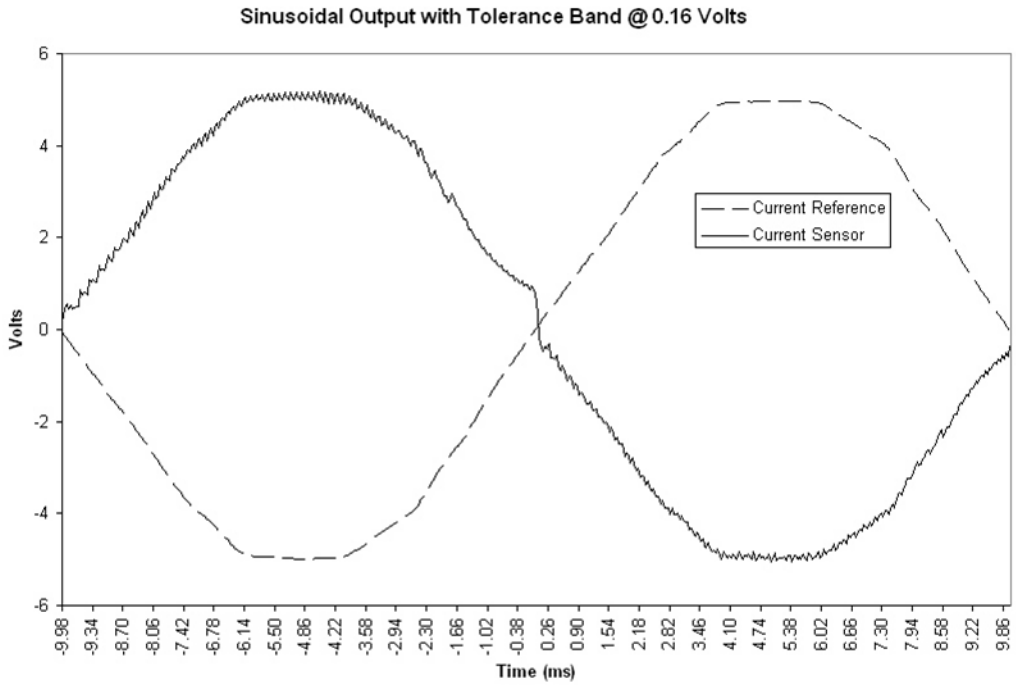


Figure 6.14: Oscilloscope image demonstrating sinusoidal output with small tolerance.

Chapter 7 PIC IMPLEMENTATION

The main objective of this project was to determine if implementation by modern electronics, such as a PIC, could optimise the original current controller. The results of the research undertaken to perform this task are outlined in this chapter.

The initial section starts with an introduction to microcontrollers in general and then focuses specifically on PIC microcontrollers. It gives details of the PIC microcontroller from its origins to the present day. The section concludes with a description of PIC hardware, software and available accessories.

The chapter continues by listing conditions that must be satisfied to ensure successful PIC implementation. An overview of available PICs that meet the requirements is discussed with the final decision being the PIC18C242. The following section lists significant characteristics of the PIC18C242 and includes the pinout diagram and description.

The chapter concludes with a flow chart, which includes sample code and execution times, designed for the PIC18C242 implemented current controller.

7.1 Introduction to PIC Microcontrollers

A microcontroller is a special type of microprocessor that integrates all the required features on a single chip to give it the versatility to control outputs with various forms of inputs. They are sometimes referred to as a single chip computer because they include all the basic computer devices such as a CPU, EPROM, RAM, I/O lines, Serial and Parallel ports, timers and built in peripherals such as A/D and D/A converters (Iovine 2004). The majority of microcontrollers range from 4 to 16-bit but the market has been dominated by the 8-bit series since the early 1990s (Peatman 1998). Microcontrollers are used in most of today's electronic equipment ranging from simple appliances such as toasters to more intricate equipment like mobile phones or computer printers. Their world wide usage is approximately 30 times larger than the computer based processor (Peatman 1998).

The PIC, or Peripheral Interface Controller, is a microcontroller designed by Microchip Technology Inc. (previously known as General Instruments). They originally designed the chip in the 1970s to reintroduce the Harvard Architecture system, which uses separate memory and buses for communication (Predko 2002). This system utilised ROM to store the instruction program and a separate RAM for instruction execution. This method equated to a much faster and efficient controller.

Today, Microchip Inc. has a complete line of PICs on the market and they classify them as 'low end', 'mid range' and 'high end'. The low end range start at simple 8-pin devices that do not include peripherals such as A/D converters and include only a simple 35-instruction set. The high end PICs come in 40 to 84-pin packages and include high levels of peripheral integration such 16 channels of 10-bit D/A converters, multi-timers, vectored interrupt handling and various serial interface capabilities (Farnell 2005). Their instruction set includes 58 single word instructions and are upward compatible with the lower end PICs.

To increase speed of execution, PICs use the technique of pipelining where an instruction is fetched from memory and ready to be executed during implementation of the previous instruction (Varley 1998). The general programming code is low-level language but there are PICs available that include and extra EEPROM, referred to as a Parallax Basic Stamp, which allow high-level coding. These chips were designed to increase coding simplicity but have the disadvantage of increasing the instruction execution time and it was for this reason that they were not suitable for the current controller design. The low-level program coding is done in the same way as standard assembly language where a basic text editor is used to write the program and an assembler compiles it. The most common assembler used for PICs is the MPASM assembler supplied by Microchip.

PIC development tools are available to give the user complete access to the PIC. These are available as either integrated boards that have various functions such as RS-232 and USB interface, code compiler and PIC program transfer, or specialist boards that carry out a single function such as EPROM erasing. Demo boards are available that allow PICs to be simulated. These boards can be used to check the PIC for correct operation and provide a way for inexperienced users to gain familiarity with PICs. Emulators are also available that give access to the internal bus lines which permit monitoring of the memory bus during program execution.

7.2 PIC Requirements for Current Controller Circuit

To ensure successful PIC implementation as the current controller, the following conditions must be satisfied by the PIC.

- **Gate switching times must be less than 200 μs.**
  The inverter gate switching can be up to 100 times the output frequency, which will be 50 Hz. This equates to a gate switching frequency of up to 5 kHz or a period of 200 μs.

- **Response time of approximately 5 µs once error reaches tolerance band.**
  The desired error reaction time is approximately 5 µs. This means that the PIC must be able to execute all instructions and change the required output within 5 µs once the error reaches the tolerance band. Although this was the desired time for the discrete component current controller circuit it should not be as critical for the PIC circuit because all the controlling will be done internally.

- **Requires 10-bit or higher A/D converters.**
  During testing of the original current controller it was demonstrated that saturation of the inverter output current occurred for tolerances below 0.16 V with a reference voltage of 10 V_{p-p}. Taking into account the gain of 20 applied to V_{tol} and the logic circuit meant a tolerance band of V_{ref} ±0.016 V. To achieve equivalent results using a PIC would require the A/D converter to have a step size of 16 mV for a 10 V_{p-p} reference voltage or $\frac{10V}{16mV} = 625$ steps. A 10-bit A/D converter provides 2^{10} or 1024 discrete steps to an analog signal. Therefore, if the V_{ref} line was set up to convert a 10 V_{p-p} range, the digital increments would be equivalent to $\frac{10V}{1024}$ or 9.77 mV. This would allow two steps either side of the reference voltage to produce an inverter output current equivalent to the original current controller circuit.

- **Requires 2×A/D converters.**
  One converter for the current reference that will also determine voltage polarity and a second converter for the bridge inverter current sensor.

- **Requires 4×digital output lines.**
  The PIC will control the states of 4 gates and will therefore require at least 4 digital outputs.

Note, that the available memory was not considered because the current controller operation was relatively simple and even the low-end chips would have ample memory. The main requirements that had to be met were speed of operation and the inclusion of A/D converters. Although the desired error reaction time was 5 μs in the original current controller, excellent results should still be obtained if the time was increased slightly.

7.3 Selecting a Suitable PIC

Before selecting a suitable PIC, it first had to be determined if any PICs were available that fulfilled the guidelines mentioned in the previous section. If it showed that PICs were not suitable then research would have to be done to find an alternative, such as DSPs (Digital Signal Processors).

With such a large range of PICs available the obvious choice was to start at the most common PIC, the PIC16Cxxx series. This range of chips varied from 20 to 24 MHz maximum clock speed, 13 to 52 I/O ports and up to 10×12-bit A/D converters (Farnell 2005). The number of I/O lines and A/D converters was substantial and so was the bit quality of the A/D converters. The only uncertainty was the maximum clock speed. For the chips containing the 12-bit A/D converters, the clock speed was 20 MHz or a period of $\frac{1}{20\times10^6}$ seconds = 50 ns. These PICs take 4 clock cycles to execute 1 instruction; therefore each instruction would take 200 ns or 0.2 μs. This only allowed 25 instructions to keep under the 5 μs target and therefore a faster operating PIC would be desired.

Inspection of the high-end PIC range revealed that the PIC17Cxxx series increased the maximum clock frequency to 33 MHz but the A/D converters were limited to 8-bit (Farnell 2005). The PIC18Cxxx offered up to 40 MHz maximum clock frequency with 10-bit A/D converters (Farnell 2005). This series had the advantage of executing an instruction in half the time of the PIC16Cxxx series but at a compromise of a reduced A/D bit sample.

An important factor to consider was the A/D conversion time. Calculations made from the data sheets for a PIC16Cxxx running with a 20 MHz clock show a conversion time of 20.8 μs while the calculated conversion time for a PIC18Cxxx running with a 40 MHz clock was only 19.2 μs. This data demonstrated that although the step size for the 12-bit A/D converter provided in the PIC16Cxxx series would be a quarter of the size of the 10-bit converter provided in the PIC18Cxxx series, it was disadvantaged by the conversion time. For this and the fact that the PIC18Cxxx could execute instructions at twice the speed of the PIC16Cxxx, it was decided that the PIC18Cxxx series was the preferred choice of PIC.

The PIC18Cxxx series consists of a number of chips but the bottom of the range chip, the PIC18C242, would be the choice for the current controller implementation. This chip has a maximum clock speed of 40 MHz, 23 I/O lines from 3×ports, and includes 5×10-bit A/D converters (Microchip PIC18Cxx2). The following section gives a detailed look at the PIC18C242 chip.

7.4 The PIC18C242

This section gives an overview of some of the PIC18C242 characteristics that will be significant for the current controller implementation. Refer to appendix C for the PIC18C242 block diagram and PIC18Cxxx instruction set. The following information was obtained from data sheets supplied by Microchip Technology Inc.

Item	**Description**
EPROM	16 kBytes Each single word instruction occupies 2 Bytes. Therefore the EPROM can store 8192 single word instructions.
RAM	512 Bytes This will be more than sufficient for the current controller circuit.

Clock	DC → 40 MHz osc/clock in At 4 cycles per instruction, this processes up to 10 million instructions per second.
I/O Ports	3×8-bit Bi-directional I/O Ports The ports can be set up to be either TTL digital I/O, analog inputs, external clock input, interrupts and various other functions.
A/D Converters	5×10-bit A/D Converters Conversion times are calculated as $12\times T_{AD}$ where T_{AD} is the conversion time per bit. The minimum recommended time to ensure accurate conversion is 1.6 μs. Therefore the minimum conversion time is 12×1.6 = 19.2 μs. T_{AD} is set in the software.
Other Features	High Current Sink/Source (25 mA/25 mA) 3×External Interrupts 4×Timers

The chip is available in the standard 28-pin DIP package as illustrated in figure 7.1. The pinout diagram is displayed in figure 7.2 with a description of each listed in table 7.1.

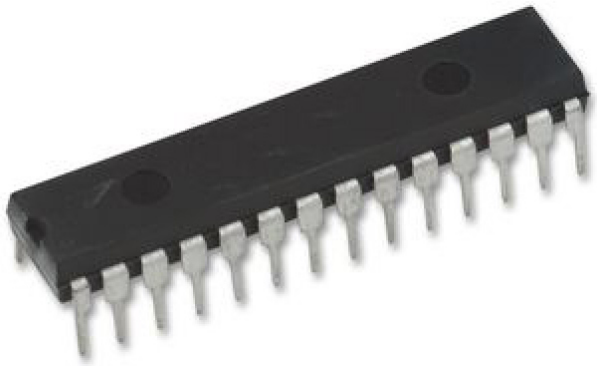


Figure 7.1: Image of PIC18C242 Chip (Microchip PIC18Cxx2).

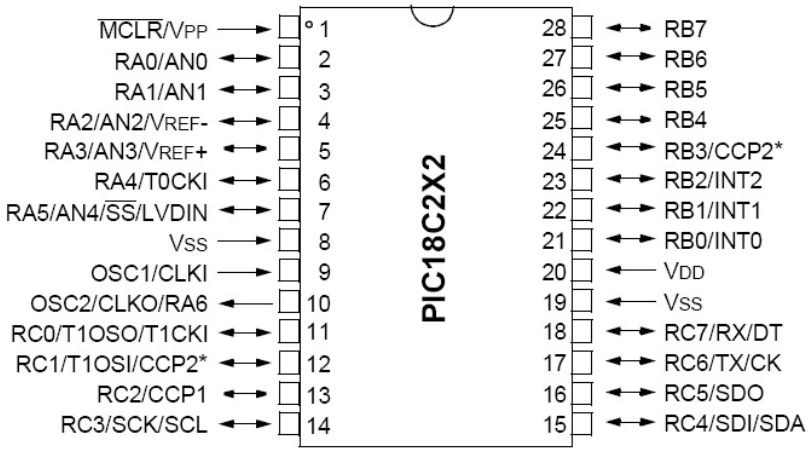


Figure 7.2: PIC18C242 Pinout Diagram (Microchip PIC18Cxx2).

Table 7.1: PIC18C242 Pinout Description (Microchip PIC18Cxx2).

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	DIP	SOIC			
MCLR/VPP	1	1			
MCLR			I	ST	Master clear (reset) input. This pin is an active low reset to the device.
VPP			P		Programming voltage input.
NC	—	—	—	—	These pins should be left unconnected.
OSC1/CLKI	9	9			
OSC1			I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. CMOS otherwise.
CLKI			I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKIN, OSC2/CLKOUT pins).
OSC2/CLKO/RA6	10	10			
OSC2			O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode.
CLKO			O	—	In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
RA6			I/O	TTL	General Purpose I/O pin.
					PORTA is a bi-directional I/O port.
RA0/AN0	2	2			
RA0			I/O	TTL	Digital I/O.
AN0			I	Analog	Analog input 0.
RA1/AN1	3	3			
RA1			I/O	TTL	Digital I/O.
AN1			I	Analog	Analog input 1.
RA2/AN2/VREF-	4	4			
RA2			I/O	TTL	Digital I/O.
AN2			I	Analog	Analog input 2.
VREF-			I	Analog	A/D Reference Voltage (Low) input.
RA3/AN3/VREF+	5	5			
RA3			I/O	TTL	Digital I/O.
AN3			I	Analog	Analog input 3.
VREF+			I	Analog	A/D Reference Voltage (High) input.
RA4/T0CKI	6	6			
RA4			I/O	ST/OD	Digital I/O. Open drain when configured as output.
T0CKI			I	ST	Timer0 external clock input.
RA5/AN4/SS/LVDIN	7	7			
RA5			I/O	TTL	Digital I/O.
AN4			I	Analog	Analog input 4.
SS			I	ST	SPI Slave Select input.
LVDIN			I	Analog	Low Voltage Detect Input.
RA6					See the OSC2/CLKO/RA6 pin.

Table 7.1 cont.

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	DIP	SOIC			
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0	21	21			
RB0			I/O	TTL	Digital I/O.
INT0			I	ST	External Interrupt 0.
RB1/INT1	22	22			
RB1			I/O	TTL	
INT1			I	ST	External Interrupt 1.
RB2/INT2	23	23			
RB2			I/O	TTL	Digital I/O.
INT2			I	ST	External Interrupt 2.
RB3/CCP2	24	24			
RB3			I/O	TTL	Digital I/O.
CCP2			I/O	ST	Capture2 input, Compare2 output, PWM2 output.
RB4	25	25	I/O	TTL	Digital I/O. Interrupt on change pin.
RB5	26	26	I/O	TTL	Digital I/O. Interrupt on change pin.
RB6	27	27	I/O	TTL	Digital I/O. Interrupt on change pin.
			I	ST	ICSP programming clock.
RB7	28	28	I/O	TTL	Digital I/O. Interrupt on change pin.
			I/O	ST	ICSP programming data.

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	DIP	SOIC			
					PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	11			
RC0			I/O	ST	Digital I/O.
T1OSO			O	—	Timer1 oscillator output.
T1CKI			I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	12	12			
RC1			I/O	ST	Digital I/O.
T1OSI			I	CMOS	Timer1 oscillator input.
CCP2			I/O	ST	Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	13	13			
RC2			I/O	ST	Digital I/O.
CCP1			I/O	ST	Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	14	14			
RC3			I/O	ST	Digital I/O.
SCK			I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL			I/O	ST	Synchronous serial clock input/output for I^2C mode
RC4/SDI/SDA	15	15			
RC4			I/O	ST	Digital I/O.
SDI			I	ST	SPI Data In.
SDA			I/O	ST	I^2C Data I/O.
RC5/SDO	16	16			
RC5			I/O	ST	Digital I/O.
SDO			O	—	SPI Data Out.
RC6/TX/CK	17	17			
RC6			I/O	ST	Digital I/O.
TX			O	—	USART Asynchronous Transmit.
CK			I/O	ST	USART Synchronous Clock. (See related RX/DT)
RC7/RX/DT	18	18			
RC7			I/O	ST	Digital I/O.
RX			I	ST	USART Asynchronous Receive.
DT			I/O	ST	USART Synchronous Data. (See related TX/CK)
VSS	8, 19	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	20	P	—	Positive supply for logic and I/O pins.

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power
OD = Open Drain (no P diode to VDD)

7.5 PIC Implemented Flow Chart and Sample Code

To demonstrate the procedure of the PIC designed current controller, a flow chart was design as illustrated in figure 7.3.

With reference to the flow chart, note the following:

- The chart refers to sensing voltages instead of currents even though this is a current controller. This is because the photovoltaic system will incorporate current sensors that are current to voltage converters.

- The voltage polarity is determined at the first decision point by the V_{ref} reading taken from the A/D converter.

- The order that the gates are energised and a 0.2 μs blanking time prevents common side transistors shorting the inverter bridge rails. The 0.2 μs blanking time is a result of the 2 instructions required to turn off the appropriate *A-side* transistor and energise the opposite *B-side* transistor. If future work illustrates that extra time is required due to gate propagation delays then all that is required would be to code a simple loop that takes the desired time to execute.

- The system will have negative feedback therefore summing V_{ref} and V_{sen} will be the same as the reference current minus the inverter output current.

- There is no need for an external tolerance band input because the tolerance will be determined in the program and set by the difference between V_{ref} and V_{sen}. The flow chart illustrates a tolerance of 2 bits either side of the reference voltage, which is equivalent to tolerance bands at V_{ref} ±0.195%.

- The process is a loop that will run continuously while the photovoltaic system is operating.

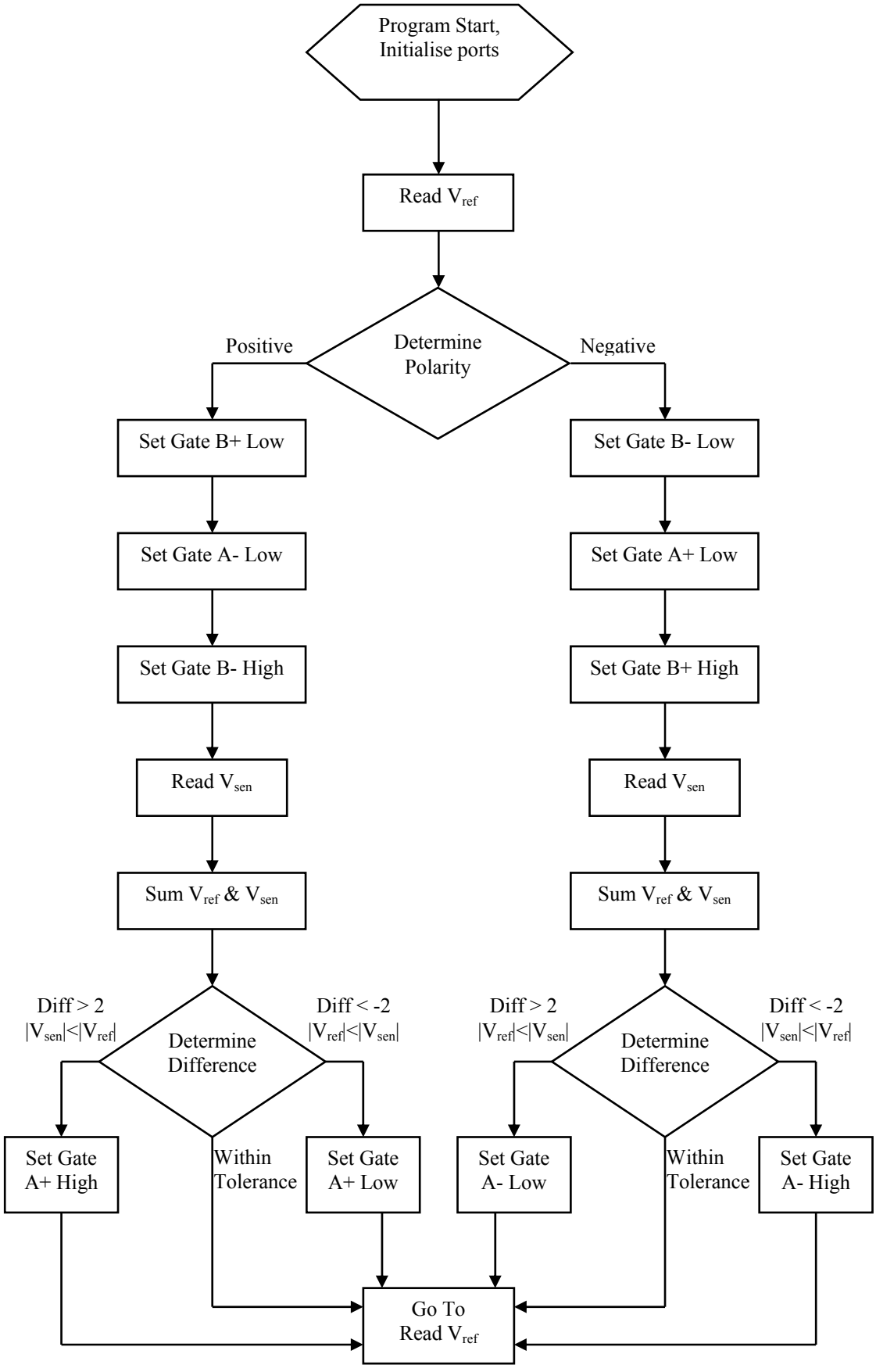


Figure 7.3: PIC Implemented Flow Chart.

A description of each process is provided in table 7.2. This table also provides sample code for each step along with instruction execution times for a PIC running at 40 MHz. The code was provided to calculate an accurate prediction of the instruction times taken throughout the current controller. To improve clarity and simplicity the sample code only demonstrates the condition for positive polarity and for V_{sen} below the tolerance band, therefore gate A+ is turned on. The complete code is displayed in appendix D.

The program was written with the use of Port A and Port B as follows:

Bit	Pin	Assignment
A0	2	A/D input for V_{ref}
A1	3	A/D input for V_{sen}
A2	4	A/D V– (-5 V reference)
A3	5	A/D V+ (+5 V reference)
B0	21	Digital output for gate B+
B1	22	Digital output for gate B-
B2	23	Digital output for gate A+
B3	24	Digital output for gate A-

Table 7.2: Flow Chart Description, Sample Code and Execution Time.

Process	Description
Program Start, Initialise Ports	The program is directed to the first program address, which is usually 0x00. The function of each port is determined. For example, what lines are assigned as digital I/O and what lines are A/D converters, and whether they are inputs or outputs.

```
      ORG   0             ;let program start at the first address 0x00
      MOVLW 0xFD          ;configure Port A
      MOVWF ADCOND1       ;set RA<3:0> as A/D inputs
                          ;let RA<0> = Vref & RA<1> = Vsen
                          ;let RA<2> = reference V-
                          ;let RA<3> = reference V+
      MOVLW 0xFF          ;value to configure data direction
      MOVWF TRISA         ;set all of port A as inputs
      CLRF  PORTB         ;initialise port B by clearing output
                          ;let RB<0> = B+ & RB<1> = B-
                          ;let RB<2> = A+ & RB<3> = A-
      MOVLW 0x00          ;value to configure data direction
      MOVWF TRISB         ;set all of port B as outputs
```

%Execution time N/A

Read V_{ref}	A digital reading is taken from the voltage applied to the A/D line assigned as the reference voltage input. Deduct 512 bits (half of the total A/D bits) from the A/D value to centre the digital reading.

```
READV MOVLW 0x85        ;configure Port A bit 0 ie. Vref
      MOVWF ADCON0      ;start A/D conversion
      MOVLW 0x200       ;load w register with 512
      SUBLW ADRESH      ;read value in A/D register and deduct 512
      MOVWF 2           ;move result in w to f register 2
```

%Execution time = 5 × 0.1 + 19.2 = 19.7 μs

Determine Polarity	The polarity is determined from the binary value of the voltage reference and the program branched to the appropriate address.

```
      BN    VNEG        ;branch to VNEG if value in w (Vref) is
                        ;negative
      BNN   VPOS        ;branch to VPOS if value in w (Vref) is
                        ;not negative
```

%Execution time = (1 or 2) × 0.1 = 0.1 or 0.2 μs

Set Initial Gate Outputs	First, the 2×transistors not used in the particular voltage cycle are de-energised and then the opposite 'B' transistor gate output is set high.

```
VPOS  BCF   PORTB,0     ;set bit 0 of port B to 0 ie. B+ to low
      BCF   PortB,3     ;set bit 3 of port B to 0 ie. A- to low
      BSF   PORTB,1     ;set bit 1 of port B to 1 ie. B- to high
```

%Execution time = 3 × 0.1 = 0.3 μs

Read V_{sen}	A digital reading is taken from the voltage applied to the A/D line assigned as the sense voltage input. Again, 512 is deducted to centre the digital reading.

```
      MOVLW 0x8D        ;configure Port A bit 1 i.e. Vsen
      MOVWF ADCON0      ;start A/D conversion
      MOVLW 0x200       ;load w register with 512
      SUBLW ADRESH      ;read value in A/D register and deduct 512
```

% Execution time = 4 × 0.1 +19.2 = 19.6 μs

Sum V_{ref} & V_{sen}	The binary values from the V_{ref} & V_{sen} readings are added. Because V_{sen} is negative, the result will be the difference.

```
      ADDWF 2           ;add value in f register 2 to W register
                        ;ie. add Vref and Vsen
                        ;and store result in f register 2
```

% Execution time = 1 × 0.1 = 0.1 μs

Determine Difference	The theoretical difference will determine which address to branch to for the appropriate 'A' gate to be controlled. The actual value will be in the 2's complement form.

```
      MOVLW 0x03        ;load w with 3
      SUBWF 2,0         ;subtract 3 from value in f register 2
      BNN   APLSH       ;branch to set gate A+ high
      MOVLW 0x02        ;load w with 2
      ADDWF 2,0         ;add 2 to value in f register 2
      BN    APLSL       ;branch to set gate A+ low
      BRA   READV       ;within tolerance so branch to read Vref
```

%Execution time = (3 or 6 or 7) × 0.1 = 0.3 or 0.6 or 0.7 μs

Set 'A' Gate Output	Depending on the voltage polarity, either the A+ or A- gates will be controlled and the result of the V_{ref} & V_{sen} sum determines whether the gate output remains the same or changed to either high or low.
`APLSH BSF PORTA,2 ;set bit 2 of port B to 1 ie. A+ to high` % Execution time = 1 × 0.1 = 0.1 μs		
Go To Read V_{ref}	To repeat the loop, the program jumps back to the V_{ref} address.
`GOTO READV ;loop back to read reference voltage` %Execution time = 0.2 μs.	

This demonstration illustrated a maximum time from initialising V_{sen} read to controlling the appropriate gate output was 20.4 μs. The following calculation illustrates what effect this time delay would have on a typical photovoltaic system. For this example, let the following conditions apply.

The inverter output voltage $V = 230 \times \sqrt{2} = 325V$

The inductive load $L = 100mH$

The change in time $dt = 20.4\mu s$

The voltage across an inductor $V = L\dfrac{di}{dt}$

$\therefore$ The change in inductor current $di = \dfrac{V}{L}dt$

Substituting in values yields $di = \dfrac{325 \times 20.4 \times 10^{-6}}{100 \times 10^{-3}} = 66.3mA$

This illustrates that the change in the inverter output current due to the time taken modifying the appropriate gate would be 66.3 mA and confirms that good results would be obtained for a PIC current controller.

The sample code demonstration also illustrated a maximum time of 40.6 μs for a complete loop. This permits more than 500 loops for every 50 Hz cycle, which is ample for the pulse width modulation technique that operates at approximately 100 times the output frequency.

With all the PIC implemented current controller requirements fulfilled, it was established that the new controller would operate successfully.

Chapter 8 DISCUSSION AND CONCLUSION

8.1 Achievement of Objectives

Referring to my project specification provided in appendix A, the objectives that I put forward changed slightly throughout the year. Firstly, testing of the current controller included temporarily constructing the gate drive circuit and a modification of the bridge inverter. The second change was that the research of implementing a PIC microcontroller into the current controller was only used as a theoretical guide and that purchasing the required equipment was not carried out due to time and money restrictions. For this reason, it was decided that I would design and construct the PCBs based on the original current controller design. With this said, a summary of the objectives that I completed included:

- Construction and testing of the original current controller system with successful results.

- Research into a PIC implemented current controller was successful and a complete program for this task was written for the PIC18C242 microcontroller.

- A PCB of the original current controller circuit was designed with 3 final boards manufactured and tested.

8.2 Further Work

There are two areas of further work that have been greatly improved as a result of this project.

The first is that further testing of the photovoltaic system, and specifically single-phase bridge inverters, can now be carried out using the current controller PCBs that I have built and tested. This will provide a quicker and more confident method of testing by eliminating the need to temporarily constructing a current controller circuit again. It will also reduce typical breadboard errors such as faulty connections and extra noise picked up on the longer connecting wires and component legs. It would be an advantage for the photovoltaic system if a future student were to design and construct a PCB of the inverter circuit.

The second is that my current controller program, provided in appendix D, could be implemented in the design and manufacturing of a PIC implemented current controller. This would involve purchasing a PIC18C242 microcontroller and appropriate development tools required to encode and test the PIC. A temporary circuit should then be constructed to test the new current controller in the photovoltaic system and if it proves to be successful, a PCB of the new current controller could be designed and manufactured.

8.3 Conclusion

The topics covered by this dissertation included the power electronics involved in switch-mode inverters, pulse-width modulation, current control techniques and gate drive circuits. It also provided a comprehensive chapter on how each section of the current controller system was tested and illustrated the results obtained. The final topic provided information about PIC microcontrollers and made a recommendation including a sample program for a PIC18C242 implemented current controller.

LIST OF REFERENCES

Fairchild Semiconductor HCPL-2503, 'High Speed Transistor Optocouplers', Fairchild Semiconductor, USA.

Farnell 2005, *Farnell Inone Electronic Engineering*, A Premier Farnell Company, NSW Australia.

Floyd, T 2002, *Electronic Devices*, 6th edn, Prentice Hall International Inc, New Jersey.

Fuji Electric, '*Gate Drive Circuit Design*', e-Front Runners, viewed 17 September 2005, <http://www.fujielectric.co.jp/eng/fdt/scd/pdf/Manual/IGBT-07.pdf>

International Rectifier IR2110/IR2113, 'High and Low Side Driver', International Rectifier, USA.

Iovine, J 2004, *PIC Microcontroller Project Book*, 2nd edn, McGraw-Hill, New York.

Lander, CW 1987, *Power Electronics*, 2nd edn, McGraw-Hill, UK.

Mazda, F 1997, *Power Electronics Handbook*, 3rd edn, Newnes, UK.

Microchip PIC18Cxx2, 'High-Performance Microcontrollers with 10-Bit A/D', Microchip Technology Inc., USA.

Mohan/Underland/Robbins, 1995, *Power Electronics Converters, Applications & Design*, 2nd edn, John Wiley & Sons, Canada.

Peatman, JB 1998, *Designing with PIC Microcontrollers*, Prentice Hall, New Jersey.

Predko, M 2002, *Programming & Customizing PICmicro Microcontrollers*, 2nd edn, McGraw-Hill, New York.

Rashid, M 1988, *Power Electronics Circuits, Devices & Applications*, 2nd edn, Prentice Hall International, London.

Varley, J 1998, *The Engineers Guide to Programming PICs*, John Varley Publications, UK.

BIBLIOGRAPHY

Ahfock, A 2004, *ELE3805 Power Electronics Principles & Applications Study Book 1 & 2*, University of Southern Queensland, Toowoomba.

International IR Rectifier IRG4BC30KD 1997, 'Insulated Gate Bipolar Transistor with Ultrafast Soft Recovery Diode', International IR Rectifier.

Microchip PIC16C717/770/771, '18/20-Pin CMOS Microcontroller 10/12-Bit A/D', Microchip Technology Inc.

Motorola 1991, *CMOS Logic Data Series C*, Technical Information Centre, USA.

National Semiconductor 2004, *Semiconductor Technical Data*, National Semiconductor Corporation.

Texas Instruments 1998, *Data Sheets from Harris Semiconductor*, Texas Instruments Inc.

Appendix A – PROJECT SPECIFICATION

University of Southern Queensland

FACULTY OF ENGINEERING AND SURVEYING

ENG 4111/4112 Research Project
PROJECT SPECIFICATION

FOR: **ALISTA MILETIC**

TOPIC: CURRENT CONTROLLER FOR INVERTER BRIDGE DESIGNED FOR GRID-CONNECTED PHOTOVOLTAIC SYSTEM

SUPERVISOR: Dr. Tony Ahfock

ENROLMENT: ENG 4111 – S1, D, 2005;
ENG 4112 – S2, D, 2005

PROJECT AIM: A grid-connected photovoltaic system includes an inverter which converts DC from the photovoltaic panels to AC. The inverter has to be controlled so that its output frequency matches that of the grid to which it is connected and its output current is near sinusoidal. The aim of this project is to optimise the existing current controller design by using programmable ICs. The final stage will be to construct a professional PCB circuit board with the new design.

PROGRAMME: **Issue A, 21st March 2005**

1. Temporarily construct and prove the existing current controller circuit.
2. Research the possibility of replacing the standard IC's with Programmable ICs (PICs) or Digital Signal Processors (DSPs) if the PIC's prove to be unsuitable.
3. Replace the temporary current controller components with the new PICs or DSPs and make the necessary adjustment required to achieve the desired output.
4. Design a PCB layout on the new circuit once it has be tested and proven.
5. Construct the final circuit board and test.

As time permits:

6. Test the existing inverter bridge circuit.
7. Design a PCB layout of the inverter bridge circuit and construct the final circuit board.

AGREED:

_____(Student) _____(Supervisor)

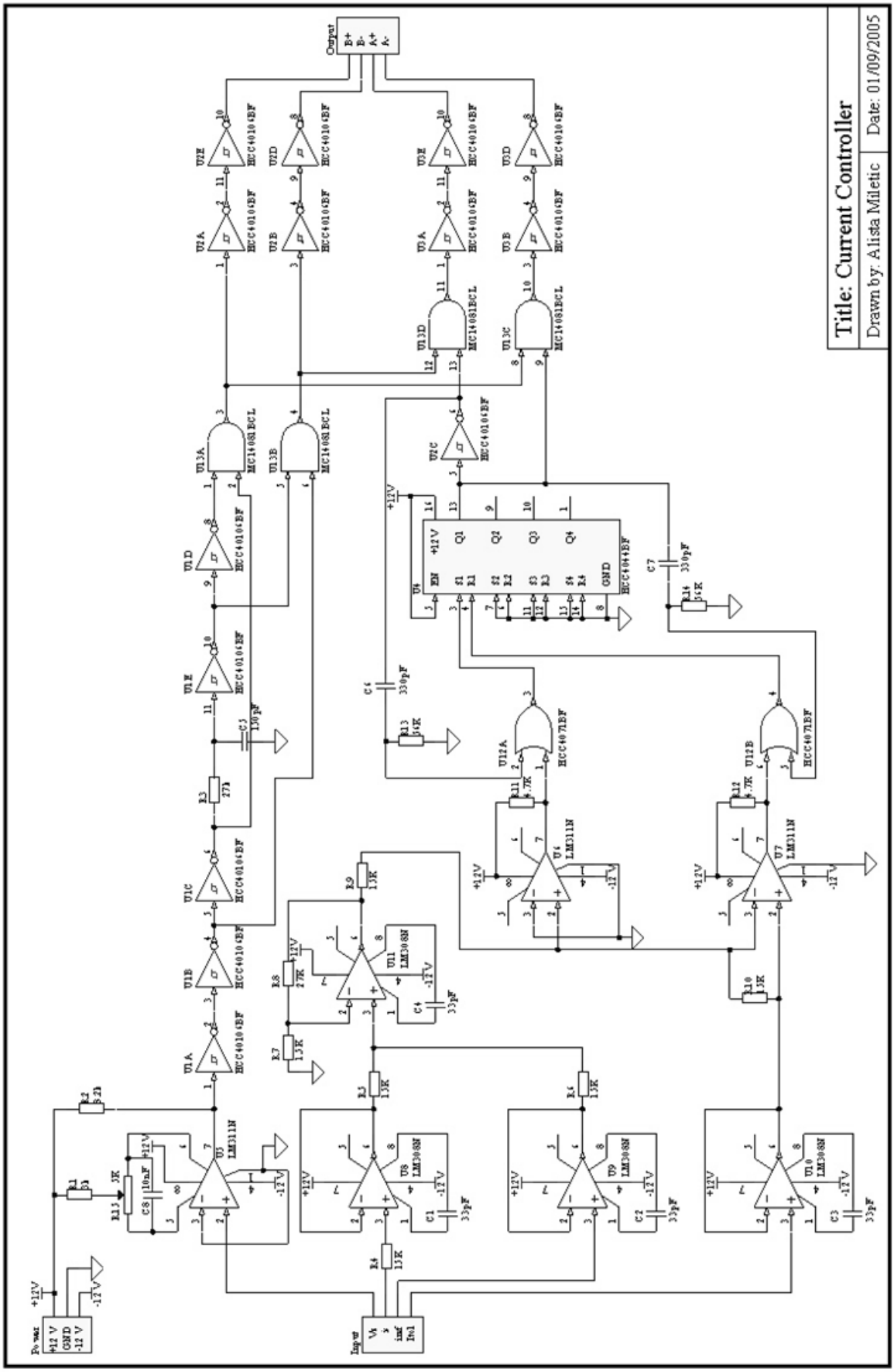
___/___/___ ___/___/___

Appendix B – CURRENT CONTROLLER SCHEMATIC AND PCB

B.1 – Current Controller Schematic

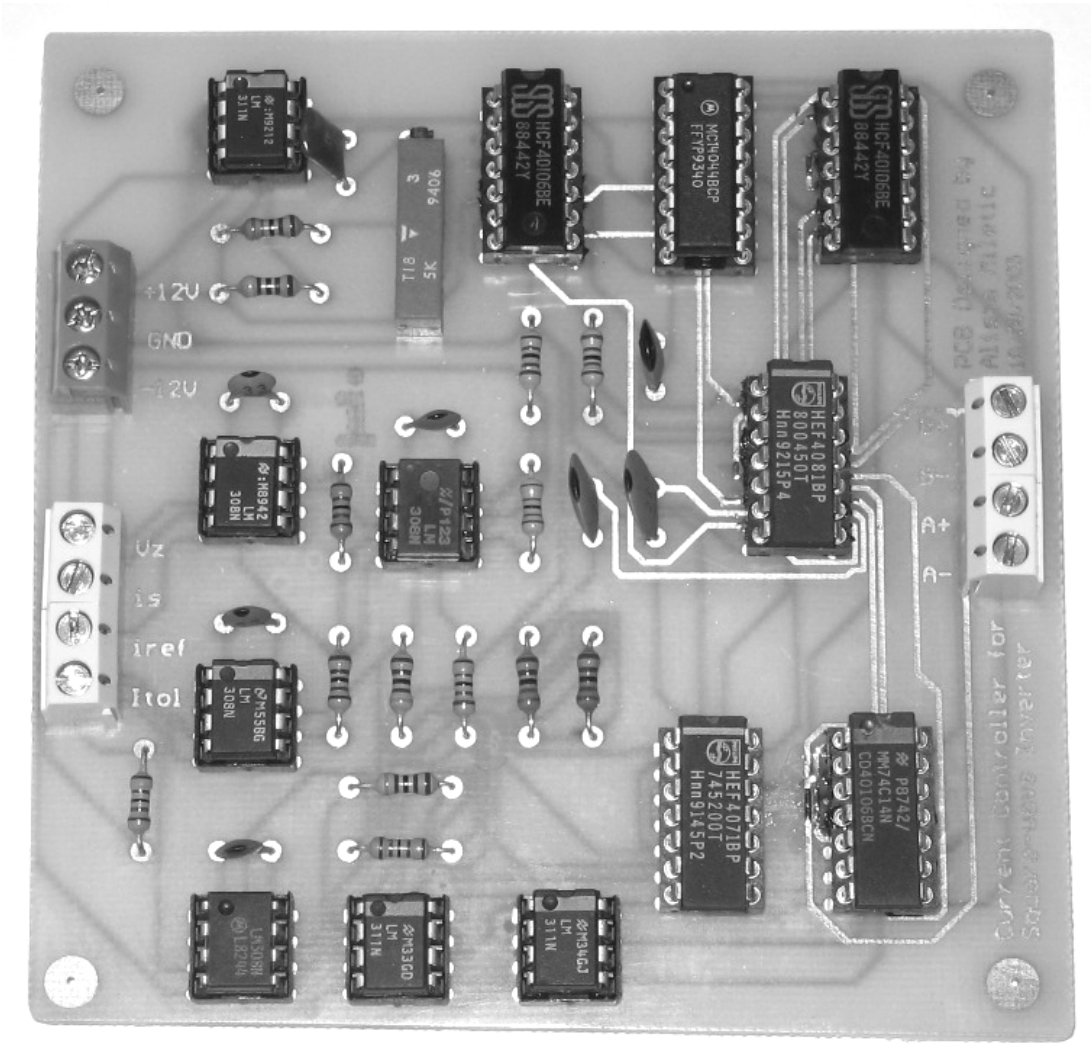
B.2 – Image of Printed Circuit Board

Appendix B.1


Title: Current Controller
Drawn by: Alista Miletic
Date: 01/09/2005

Appendix B.2

Current Controller PCB



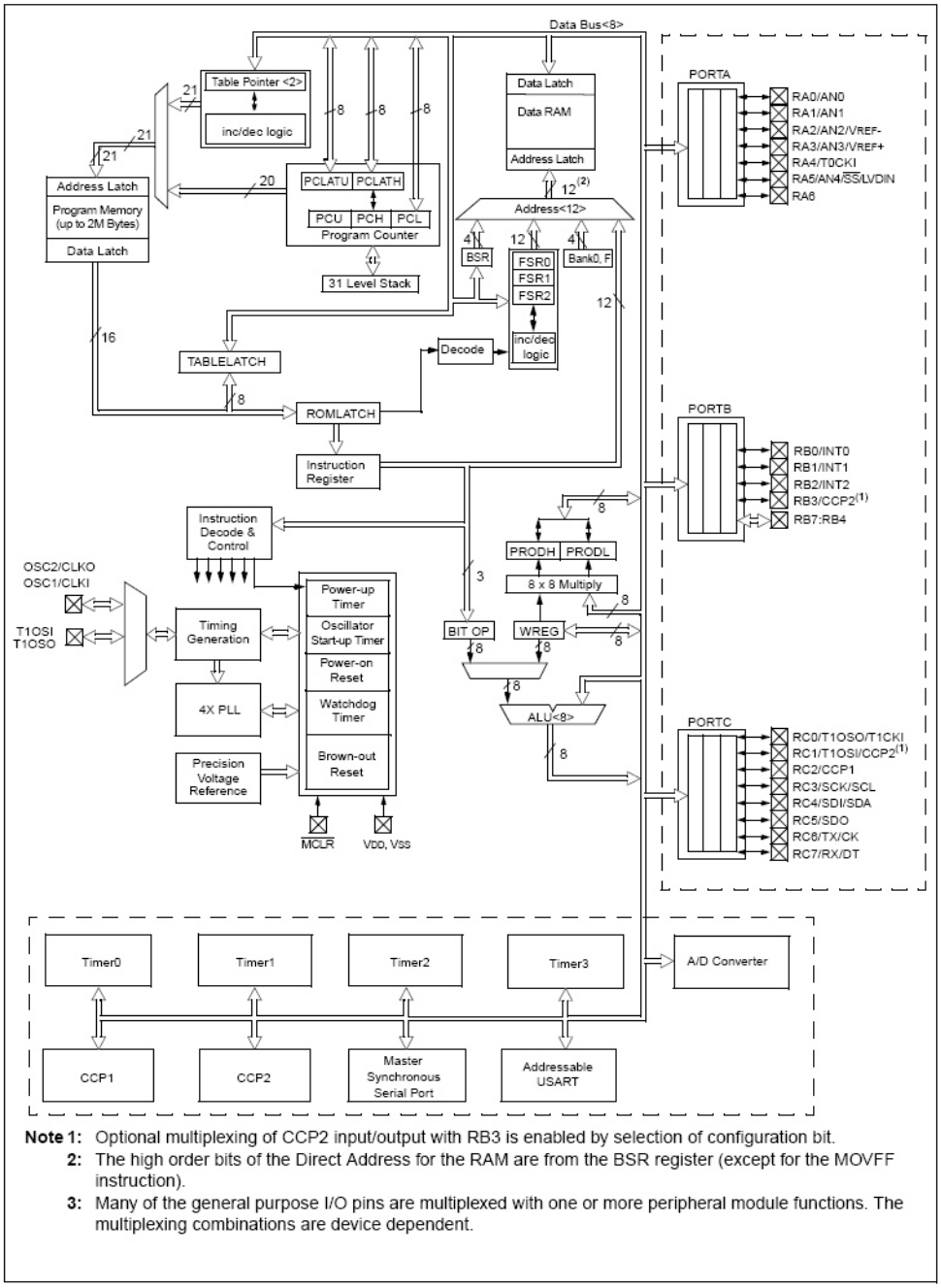
Appendix C – PIC18C242 BLOCK DIAGRAM AND INSTRUCTION SET

C.1 – PIC18C242 Block Diagram (Microchip PIC18Cxx2)

C.2 – PIC18Cxxx Instruction Set (Microchip PIC18Cxx2)

Appendix C.1

PIC18C242 Block Diagram



Note 1: Optional multiplexing of CCP2 input/output with RB3 is enabled by selection of configuration bit.

2: The high order bits of the Direct Address for the RAM are from the BSR register (except for the MOVFF instruction).

3: Many of the general purpose I/O pins are multiplexed with one or more peripheral module functions. The multiplexing combinations are device dependent.

Appendix C.1

PIC18Cxxx Instruction Set

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word MSb	LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	f, d, a	Add WREG and f	1	0010 01da ffff ffff		C, DC, Z, OV, N	1, 2
ADDWFC	f, d, a	Add WREG and Carry bit to f	1	0010 00da ffff ffff		C, DC, Z, OV, N	1, 2
ANDWF	f, d, a	AND WREG with f	1	0001 01da ffff ffff		Z, N	1,2
CLRF	f, a	Clear f	1	0110 101a ffff ffff		Z	2
COMF	f, d, a	Complement f	1	0001 11da ffff ffff		Z, N	1, 2
CPFSEQ	f, a	Compare f with WREG, skip =	1 (2 or 3)	0110 001a ffff ffff		None	4
CPFSGT	f, a	Compare f with WREG, skip >	1 (2 or 3)	0110 010a ffff ffff		None	4
CPFSLT	f, a	Compare f with WREG, skip <	1 (2 or 3)	0110 000a ffff ffff		None	1, 2
DECF	f, d, a	Decrement f	1	0000 01da ffff ffff		C, DC, Z, OV, N	1, 2, 3, 4
DECFSZ	f, d, a	Decrement f, Skip if 0	1 (2 or 3)	0010 11da ffff ffff		None	1, 2, 3, 4
DCFSNZ	f, d, a	Decrement f, Skip if Not 0	1 (2 or 3)	0100 11da ffff ffff		None	1, 2
INCF	f, d, a	Increment f	1	0010 10da ffff ffff		C, DC, Z, OV, N	1, 2, 3, 4
INCFSZ	f, d, a	Increment f, Skip if 0	1 (2 or 3)	0011 11da ffff ffff		None	4
INFSNZ	f, d, a	Increment f, Skip if Not 0	1 (2 or 3)	0100 10da ffff ffff		None	1, 2
IORWF	f, d, a	Inclusive OR WREG with f	1	0001 00da ffff ffff		Z, N	1, 2
MOVF	f, d, a	Move f	1	0101 00da ffff ffff		Z, N	1
MOVFF	f_s, f_d	Move f_s (source) to 1st word f_d (destination)2nd word	2	1100 ffff ffff ffff 1111 ffff ffff ffff		None	
MOVWF	f, a	Move WREG to f	1	0110 111a ffff ffff		None	
MULWF	f, a	Multiply WREG with f	1	0000 001a ffff ffff		None	
NEGF	f, a	Negate f	1	0110 110a ffff ffff		C, DC, Z, OV, N	1, 2
RLCF	f, d, a	Rotate Left f through Carry	1	0011 01da ffff ffff		C, Z, N	
RLNCF	f, d, a	Rotate Left f (No Carry)	1	0100 01da ffff ffff		Z, N	1, 2
RRCF	f, d, a	Rotate Right f through Carry	1	0011 00da ffff ffff		C, Z, N	
RRNCF	f, d, a	Rotate Right f (No Carry)	1	0100 00da ffff ffff		Z, N	
SETF	f, a	Set f	1	0110 100a ffff ffff		None	
SUBFWB	f, d, a	Subtract f from WREG with borrow	1	0101 01da ffff ffff		C, DC, Z, OV, N	1, 2
SUBWF	f, d, a	Subtract WREG from f	1	0101 11da ffff ffff		C, DC, Z, OV, N	
SUBWFB	f, d, a	Subtract WREG from f with borrow	1	0101 10da ffff ffff		C, DC, Z, OV, N	1, 2
SWAPF	f, d, a	Swap nibbles in f	1	0011 10da ffff ffff		None	4
TSTFSZ	f, a	Test f, skip if 0	1 (2 or 3)	0110 011a ffff ffff		None	1, 2
XORWF	f, d, a	Exclusive OR WREG with f	1	0001 10da ffff ffff		Z, N	
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	f, b, a	Bit Clear f	1	1001 bbba ffff ffff		None	1, 2
BSF	f, b, a	Bit Set f	1	1000 bbba ffff ffff		None	1, 2
BTFSC	f, b, a	Bit Test f, Skip if Clear	1 (2 or 3)	1011 bbba ffff ffff		None	3, 4
BTFSS	f, b, a	Bit Test f, Skip if Set	1 (2 or 3)	1010 bbba ffff ffff		None	3, 4
BTG	f, d, a	Bit Toggle f	1	0111 bbba ffff ffff		None	1, 2

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word MSb	LSb	Status Affected	Notes
CONTROL OPERATIONS							
BC	n	Branch if Carry	1 (2)	1110 0010 nnnn nnnn		None	
BN	n	Branch if Negative	1 (2)	1110 0110 nnnn nnnn		None	
BNC	n	Branch if Not Carry	1 (2)	1110 0011 nnnn nnnn		None	
BNN	n	Branch if Not Negative	1 (2)	1110 0111 nnnn nnnn		None	
BNOV	n	Branch if Not Overflow	1 (2)	1110 0101 nnnn nnnn		None	
BNZ	n	Branch if Not Zero	2	1110 0001 nnnn nnnn		None	
BOV	n	Branch if Overflow	1 (2)	1110 0100 nnnn nnnn		None	
BRA	n	Branch Unconditionally	1 (2)	1101 0nnn nnnn nnnn		None	
BZ	n	Branch if Zero	1 (2)	1110 0000 nnnn nnnn		None	
CALL	n, s	Call subroutine1st word 2nd word	2	1110 110s kkkk kkkk 1111 kkkk kkkk kkkk		None	
CLRWDT	—	Clear Watchdog Timer	1	0000 0000 0000 0100		$\overline{TO}$, $\overline{PD}$	
DAW	—	Decimal Adjust WREG	1	0000 0000 0000 0111		C	
GOTO	n	Go to address1st word 2nd word	2	1110 1111 kkkk kkkk 1111 kkkk kkkk kkkk		None	
NOP	—	No Operation	1	0000 0000 0000 0000		None	
NOP	—	No Operation (Note 4)	1	1111 xxxx xxxx xxxx		None	
POP	—	Pop top of return stack (TOS)	1	0000 0000 0000 0110		None	
PUSH	—	Push top of return stack (TOS)	1	0000 0000 0000 0101		None	
RCALL	n	Relative Call	2	1101 1nnn nnnn nnnn		None	
RESET		Software device RESET	1	0000 0000 1111 1111		All	
RETFIE	s	Return from interrupt enable	2	0000 0000 0001 000s		GIE/GIEH, PEIE/GIEL	
RETLW	k	Return with literal in WREG	2	0000 1100 kkkk kkkk		None	
RETURN	s	Return from Subroutine	2	0000 0000 0001 001s		None	
SLEEP	—	Go into standby mode	1	0000 0000 0000 0011		$\overline{TO}$, $\overline{PD}$	

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
				MSb			LSb		
LITERAL OPERATIONS									
ADDLW	k	Add literal and WREG	1	0000	1111	kkkk	kkkk	C, DC, Z, OV, N	
ANDLW	k	AND literal with WREG	1	0000	1011	kkkk	kkkk	Z, N	
IORLW	k	Inclusive OR literal with WREG	1	0000	1001	kkkk	kkkk	Z, N	
LFSR	f, k	Move literal (12-bit)1st word to FSRx2nd word	2	1110 1111	1110 0000	00ff kkkk	kkkk kkkk	None	
MOVLB	k	Move literal to BSR<3:0>	1	0000	0001	0000	kkkk	None	
MOVLW	k	Move literal to WREG	1	0000	1110	kkkk	kkkk	None	
MULLW	k	Multiply literal with WREG	1	0000	1101	kkkk	kkkk	None	
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
SUBLW	k	Subtract WREG from literal	1	0000	1000	kkkk	kkkk	C, DC, Z, OV, N	
XORLW	k	Exclusive OR literal with WREG	1	0000	1010	kkkk	kkkk	Z, N	
DATA MEMORY ↔ PROGRAM MEMORY OPERATIONS									
TBLRD*		Table Read	2	0000	0000	0000	1000	None	
TBLRD*+		Table Read with post-increment		0000	0000	0000	1001	None	
TBLRD*-		Table Read with post-decrement		0000	0000	0000	1010	None	
TBLRD+*		Table Read with pre-increment		0000	0000	0000	1011	None	
TBLWT*		Table Write	2 **(5)**	0000	0000	0000	1100	None	
TBLWT*+		Table Write with post-increment		0000	0000	0000	1101	None	
TBLWT*-		Table Write with post-decrement		0000	0000	0000	1110	None	
TBLWT+*		Table Write with pre-increment		0000	0000	0000	1111	None	

Note 1: When a PORT register is modified as a function of itself (e.g., `MOVF PORTB, 1, 0`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

4: Some instructions are 2 word instructions. The second word of these instruction will be executed as a `NOP`, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.

5: If the table write starts the write cycle to internal memory, the write will continue until terminated.

Appendix D – PIC18C242 CURRENT CONTROLLER CODE

PIC18C242 Sample Code, wholly written by Alista Miletic

```
        ORG   0             ;let program start at the first address 0x00
        MOVLW 0xFD          ;configure Port A
        MOVWF ADCOND1       ;set RA<3:0> as A/D inputs
                            ;let RA<0> = Vref & RA<1> = Vsen
                            ;let RA<2> = reference V-

                            ;let RA<3> = reference V+
        MOVLW 0xFF          ;value to configure data direction
        MOVWF TRISA         ;set all of port A as inputs
        CLRF  PORTB         ;initialise port B by clearing output
                            ;let RB<0> = B+ & RB<1> = B-
                            ;let RB<2> = A+ & RB<3> = A-
        MOVLW 0x00          ;value to configure data direction
        MOVWF TRISB         ;set all of port B as outputs

READV   MOVLW 0x85          ;configure Port A bit 0 ie. Vref
        MOVWF ADCON0        ;start A/D conversion
        MOVLW 0x200         ;load w register with 512
        SUBLW ADRESH        ;read value in A/D register and deduct 512
        MOVWF 2             ;move result in w to f register 2

        BN    VNEG          ;branch to VNEG if value in w (Vref) is
                            ;negative
        BNN   VPOS          ;branch to VPOS if value in w (Vref) is
                            ;not negative

VNEG    BCF   PORTB,1       ;set bit 1 of port B to 0 ie. B- to low
        BCF   PortB,2       ;set bit 2 of port B to 0 ie. A+ to low
        BSF   PORTB,0       ;set bit 0 of port B to 1 ie. B+ to high

        MOVLW 0x8D          ;configure Port A bit 1 ie. Vsen
        MOVWF ADCON0        ;start A/D conversion
        MOVLW 0x200         ;load w register with 512
        SUBLW ADRESH        ;read value in A/D register and deduct 512

        ADDWF 2,1           ;add value in f register 2 to W register
                            ;ie. add Vref and Vsen
                            ;and store result in f register 2

        MOVLW 0x03          ;load w with 3
        SUBWF 2,0           ;subtract 3 from value in f register 2
        BNN   ANEGL         ;branch to set gate A- low
        MOVLW 0x02          ;load w with 2
        ADDWF 2,0           ;add 2 to value in f register 2
        BN    ANEGH         ;branch to set gate A- high
        BRA   READV         ;within tolerance so branch to read Vref

VPOS    BCF   PORTB,0       ;set bit 0 of port B to 0 ie. B+ to low
        BCF   PortB,3       ;set bit 3 of port B to 0 ie. A- to low
        BSF   PORTB,1       ;set bit 1 of port B to 1 ie. B- to high

        MOVLW 0x8D          ;configure Port A bit 1 ie. Vsen
        MOVWF ADCON0        ;start A/D conversion
        MOVLW 0x200         ;load w register with 512
        SUBLW ADRESH        ;read value in A/D register and deduct 512

        ADDWF 2,1           ;add value in f register 2 to W register
                            ;ie. add Vref and Vsen
                            ;and store result in f register 2
```

```
       MOVLW 0x03        ;load w with 3
       SUBWF 2,0         ;subtract 3 from value in f register 2
       BNN   APLSH       ;branch to set gate A+ high
       MOVLW 0x02        ;load w with 2
       ADDWF 2,0         ;add 2 to value in f register 2
       BN    APLSL       ;branch to set gate A+ low
       BRA   READV       ;within tolerance so branch to read Vref

ANEGH  BSF   PORTB,3     ;set bit 3 of port B to 1 ie. A- to high
       GOTO  READV       ;loop back to read reference voltage
ANEGL  BCF   PORTB,3     ;set bit 3 of port B to 0 ie. A- to high
       GOTO  READV       ;loop back to read reference voltage
APLSH  BSF   PORTB,2     ;set bit 2 of port B to 1 ie. A+ to high
       GOTO  READV       ;loop back to read reference voltage
APLSL  BCF   PORTB,2     ;set bit 2 of port B to 0 ie. A+ to high
       GOTO  READV       ;loop back to read reference voltage
```

Appendix E – GLOSSARY OF TERMS

Bipolar – With respect to voltage: Is of dual polarity.

BJT (Bipolar Junction Transistor) – A transistor constructed with three doped semiconductor regions separated by two *pn* junctions (Floyd 2002).

Gate Driver – A device used to supply adequate voltage and current to ensure successful switching of power devices at high speed.

IGBT (Insulated Gate Bipolar Transistor) – A hybrid power semiconductor device which combines the low saturation voltage of a bipolar transistor with the low input current requirements of a unipolar transistor (Mazda 1997).

Inverter – A converter that changes a DC input to an AC output.

MOSFET (Metal Oxide Semiconductor Field Effect Transistor) – A voltage controlled form of unipolar transistor capable of operating in enhanced or depletion mode.

Optocoupler – An optically coupled high speed transistor IC used to isolate electrical signals.

Photovoltaic Cells – Transducers that converters radiant energy into electrical energy.

PIC (Peripheral Interface Controller) – A microcontroller designed by Microchip Technology Inc. (previously known as General Instruments).

Power Grid – The major electrical network that supplies power to domestic, commercial and industrial areas.

PWM (Pulse-width modulation) – A method for varying the mark-to-space ratio of the output voltage waveform during a cycle so as to minimise the magnitudes of the harmonics (Mazda 1997).

Unipolar – With respect to voltage: Is of single polarity.