University of Southern Queensland

School of Engineering

An Investigation into the Impact Different Quantities of Vias have on the Reliability of PCB Circuits

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Abstract

In Printed Circuit Board (PCB) design and manufacturing, there are several official and unofficial design rules; one of these unofficial design rules is via minimisation, which is to keep the number of vias in use to a minimum, potentially reducing performance and reliability loss. Vias are holes drilled into a PCB, plated typically with copper to interconnect the conductive layers of a PCB. With rising component and circuit density on PCBs, which has facilitated the increased use of vias in PCB design, it is undetermined if this overall increase in vias impacts the overall reliability of PCB circuits, consequently impacting failure rates which sequentially leads to an impact on electronic waste.

This project investigated and analysed results gathered from two physical experimentations to observe the impact that different quantities of vias have on a PCB circuit's reliability to validate or invalidate the design rule via minimisation. The focus areas were the maximum current capabilities of the circuits, and the thermal and physical properties. To conduct the experiments, three circuit types were designed and manufactured based on the different quantities of vias; the first circuit contained one via, which was the control circuit for the experiment and results; the second circuit contained five vias; and the third circuit contained ten vias. Each PCB contained twenty circuits and was all manufactured by JLCPCB, 80 circuits of each type underwent experimentation under two methodologies; the first experiment focused on the maximum current, which started at 500 mA and increased by 100mA every 5 seconds until failure, and the second experiment which had a focus on the thermal properties started at 5 A, increasing by 500mA every 20 seconds until failure, where physical and thermal images were taken in the 20-second pause. The results and images were analysed and compared between the three different circuit types.

Results show that an increased quantity of vias reduced the overall maximum current of the circuit, the circuits had a higher temperature, and the area of damage after failure was far greater, concluding that this increase is detrimental to the reliability of the circuits and validating the design rule of via minimisation. While overall detrimental, there were some benefits; the ten via circuits held higher temperatures longer than the other two circuits, and comparing the five and ten via, the temperature did not change drastically at the lower current levels.

Acknowledgments

Throughout the process of this project, I have received support and assistance.

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Table of Contents

List of Figures

List of Tables

List of Appendices

Nomenclature and Acronyms

The following abbreviations have been used throughout the literature review:

AC	Alternating Current
CPU	Central Processing Unit
DC	Direct Current
FR-4	Flame Retardant-4
GND	Ground
IC	Integrated Circuit
IPA	Isopropyl Alcohol
IPC	Association Connecting Electronics Industries®
KCL	Kirchhoff's Current Law
MCM	Multichip module
PCB	Printed Circuit Board
PPE	Personal Protective Equipment
PTH	Plated Through Hole
TSV	Through Silicon Via
SDS	Safety Data Sheet
UniSQ	University of Southern Queensland
USB	Universal Serial Bus
VLSI	Very Large-Scale Integration

Chapter 1

Introduction

1.1 Problem Identified

In Printed Circuit Board (PCB) design, there are many informal and formal design rules that cover the routing of conducting traces between components, the positioning of components, the allowed dimension of interconnection, traces, vias and pads(Elliot & Brown, 2023). One common design constraint is to minimise the quantity of vias, although, with the need for more component density and miniaturisation of PCBs increasing the need for vias, this constraint is not universally accepted or applied. The rationale can vary based on the sources in (Lienig & Scheible, 2020); via minimisation is desired as interconnections between conductive layers can impose performance and reliability loss, in (Montrose, 2000) it is to reduce and maintain trace impedance. This dissertation investigates the validity of the informal design rule of via minimisation. Vias are one integral part of PCB design, and the validity of the design rule will impact the overall optimisation of PCB designs; optimisation in the design phase consecutively impacts the reliability of PCBs which sequentially leads to an impact on electronic waste.

1.2 Background

1.2.1 PCB, Interconnections and Vias

A PCB is a low-cost platform that electrically interconnects electrical, mechanical, and thermal components, which are manufactured with alternating layers, a conductive layer and dielectric layers; the layers are shown below in Figure 1.1; the number of layers designated to a PCB is determined by the number of conductive layers (Bogatin, 2021). The conductive layer is typically made with copper foils, while the dielectric is predominantly made of a flame-retardant material such as a glass-reinforced epoxy laminated (FR-4) (Beng et al., 2013). The interconnection between components is achieved by utilising interconnection traces or tracks made of conductive material typically copper placed on the copper foils; the electrical characteristics are determined by their physical dimensions like the width, length and thickness (Bogatin, 2021). PCB pads are an uncovered conductive metal area, either surface mount or

through-hole on a PCB, used to interconnect external components to a PCB through soldering; pads can come in various shapes based on the component being connected (Bogatin, 2021). Interconnection between the copper layers is achieved by utilising vias.

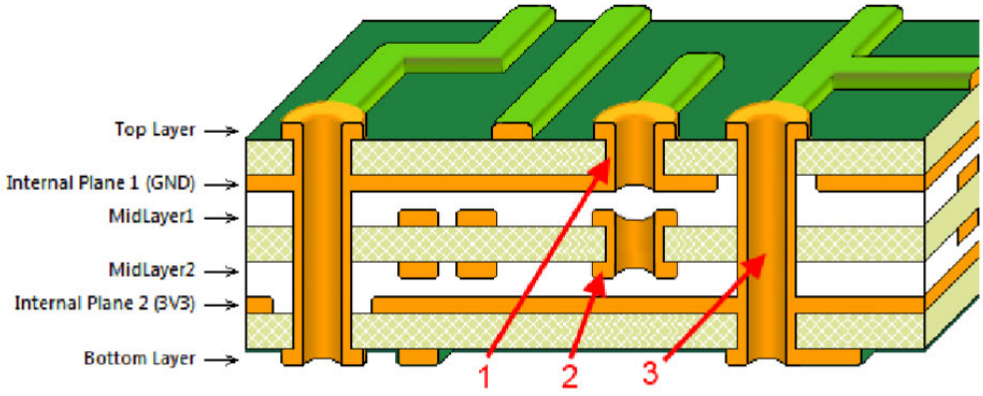

Figure 1.1: Examples of the layers that make up a 4-layer PCB and the three different types of vias: (1) blind via, (2) buried via and (3) through hole vias. Image sourced from (Bogatin, 2021).

Vias main purpose is to provide an electrical path between conducting layers; vias are holes drilled through the dielectric layers either with mechanical drills or precision lasers based on the size of the hole; the holes are then plated with a conductive material (typically copper) (Bogatin, 2021). Vias come in three major types: Buried vias connect two adjacent layers, typically internal layers; Blind are drilled to a controlled depth to connect the desired layers; and plated through-hole (PTH) being the most common is a hole drilled through the entire board, which will connect all layers through the board, these can be seen in Figure 1.1 above (Bogatin, 2021).

While vias are primarily used as an interconnection for electrical paths between PCB layers in PCB design, they have another purpose in conducting heat between layers; there are two types of vias used for their thermal properties: thermal and thermal relief. Thermal vias are typically connected to components to provide a low thermal resistance between the components and layers; these vias act as heat spreaders, spreading the heat through multiple layers of the PCB FR-4 dielectric, providing a greater area for the heat to dissipate through conduction based on Equation 1.1 (Bogatin, 2021; Moaveni, 2019).

$$Q = kA\frac{(T_1 - T_2)}{L} \quad (1.1)$$

Where: Q is the heat energy (J)

k is the thermal conductivity (W/(m * °C)

A is the cross-sectional (m^2)

L is the material thickness (m)

T1 – T2 is the temperature difference across the material (°C)

Thermal relief vias are used to limit the heat conduction of a desired electrical connection; this is done by using larger vias with narrow tabs, which provide low electrical resistance but increase thermal resistance (Bogatin, 2021). The electrical and thermal properties of a via are determined by several factors: its geometric properties, specifically its cross-sectional area, the conductive material, the manufacturing process, and the connection between the vias and interconnection traces (Bogatin, 2021).

1.2.2 Sustainability and Reliability

One of the biggest concerns around electronics is the amount of e-waste that is produced each year; the amount of e-waste that is produced grows, as shown in Figure 1.2; e-waste can come from multiple avenues, from the yearly replacement of technology such as mobile phones, end of life of a product, out-of-date technology and failure from the reliability of the electronics (Arya & Kumar, 2022). The sustainability of electronics can be improved through several means, including regular maintenance, easily replaceable components, and recycling of components and materials, furthermore can be improved by utilising effect design rules and standards in the design and manufacturing stage of its lifecycle (Patti, 2023).

Figure 1.2: Quantity of e-waste generated globally (Palanisamy & Subburaj, 2023).

Reliability in electronics and PCBs can be impacted by a variety of sources, including defects in manufacturing, contaminants on the electronics such as dust or water, mechanical components such as switches, and passive components such as resistors; one of the concerns with via is by adding them to the circuit they can behave like a passive component and in turn reduce the reliability of the circuit(van Driel et al., 2024). Reduction in reliability can lead to circuit failure and, in turn, failure of the PCB. The most common form of failure in PCBs comes from the power loss of the circuit due to the current and resistance; this is known as Joule's law, which can be explained by Equation 1.2, as the resistance or current increases the more power is loss, this power takes the form of temperature, so as the power increases the temperature of the circuit increases (Scherz & Monk, 2016). Furthermore, reliability will be impacted by how well a circuit can manage the temperature by its ability to dissipate the heat energy into surrounding material based on Equation 1.1.

$$P = I^2R \quad (1.2)$$

Where: P is the power (W);
I is the current (A);
R is the resistance (Ω)

1.3 Aim, Scope, and Objectives

The main aim of this dissertation is *to investigate the design rule of via minimization in PCB manufacturing by observing the impacts that the quantity of vias has on the reliability of PCB circuits*. The scope of the dissertation is to conduct physical experimentation on manufactured PCB circuits with different quantities of vias, observe the impacts the quantity of vias has on the maximum current, thermal properties, and physical properties of the circuits, and then come to a conclusion if the design rule is valid and provide some recommendations on using vias efficiently in PCB design to increase reliability consequently increasing the sustainability of the PCB.

Specific Objectives:

- Conduct research on the impacts vias have on a PCB circuit.
- Conduct to-failure experimentation through over-current on PCB circuits with different quantities of vias to determine the maximum current, thermal and physical properties of the circuits.
- Analysis of the data collected from the experimentation to determine the impact the quantity of vias has on the reliability of the circuits
- Conduct a comparison between the analysed data based on the quantity of vias to determine if there is a noticeable difference between the circuits.
- Conclude if the quantity of vias either is detrimental to the reliability of PCB circuits validating the design rule of via minimisation or is beneficial to the reliability of PCB circuits invalidating the design rule.
- Provide recommendations in PCB design by using vias based on the results.

1.4 Overview of the Dissertation

The dissertation is organised into the following chapters:

Chapter 1: Introduces the identified problem, background, objectives, expected outcomes and benefits of the dissertation.

Chapter 2: Literature review provides background information on recent research in PCB design, interconnectivity and reliability and critically reviews methodologies utilised in experiments from other literature.

Chapter 3: Describes the methodology used to address the identified problem of the dissertation and to meet the aim and objectives of the dissertation.

Chapter 4: Discusses the results of the methodology and analyses the results to address the objectives of the dissertation.

Chapter 5: Concludes the dissertation, provides recommendations, discusses how the dissertation is beneficial to engineering and suggests further work in the following areas: manufacturing, dimensions, crosstalk, and resistance measurements.

Chapter 2

Literature Review

2.1 Introduction

This chapter will review the literature to establish the need, feasibility, methodology and expectations of the dissertation analysis to meet the aim *to investigate the design rule of via minimization in PCB manufacturing by observing the impacts that the quantity of vias has on the reliability of PCB circuits*. Currently, there is no directly related literature that is concerned with via minimisation and reliability, and the literature covered in this chapter is loosely based on the project's objectives and broken down into the following topics:

- Via minimisation
- PCB Current and thermal capabilities
- PCB trace current and thermal capabilities
- PCB via current capabilities
- PCB Via and FR-4 Thermal capabilities
- PCB Combined Trace and Vias capabilities
- IPC Standards
- Reliability

2.2 Via minimisation

The central theme for this dissertation is investigating the design rule via minimisation and there is limited current literature that focuses on via minimisation. Looking at Very Large-Scale Integration (VSLI) in multi-layered Integrated circuits (ICs), PCBs, and Multichip Modules (MCM) (Chin-Chih & Cong, 1999), develop an algorithm that uses ECC graphs for layer assignments with a focus on via minimisation. Continuing more specifically towards VLSI in PCBs (Yan, 2021), algorithms for layer assignments were also developed with a focus on via minisuction, utilising fuzzy-cluster net assignments. Furthermore, (Chin-Chih & Cong, 1999) and (Yan, 2021) have vastly different objectives compared to this dissertation; the algorithms developed are focused on following the design rule via minimisation, compared to investigating

the validity of the design rule, neither also consider the electrical aspect of the vias; the determining factor for both was the time it took the Central Processing Unit (CPU) to reduce to the optimal number of vias to PCB layers. An approach to complying with the design rule of via minimisation is to use alternative means, by Finite Element Analysis (FEA) simulations and experimentation conducted by (Lope et al., 2015), investigate using planar coils with litz-wire structure as an implementation into reducing the quantity of vias. (Lope et al., 2015) concluded from the research that it was theoretically possible to reduce the minimum number of vias by half utilising the planar coil with Litz-wire structure; this was done on the principle of high cost compared to reliability.

The literature for via minimisation is solely focused on the reduction of the number of vias, demonstrating the importance of the design rule; because of the importance of the rule and there is no direct literature, there is room for an investigation into the impacts on reliability by the quantity of vias.

2.3 PCB Current and Thermal Capabilities

Two important factors in PCB design, manufacturing, usage, and reliability are the interconnections current and thermal capabilities. When current flows through a medium, there is also an associated thermal consideration due to power losses based on Joule's law (Equation 1.2); these two capabilities tend to be linked in the literature or are focused on the single aspects of the components, interconnections or capability of PCBs.

2.3.1 PCB Trace Current and Thermal Capabilities

Traces are the primary means of interconnection on a PCB between components; there has been a limited number of works of literature that have conducted research on the current and thermal capabilities of traces. To investigate methods to improve the current and thermal capability of traces (K R & Kumar, 2019) conducted a simulation using ANSYS workbench based on different PCB dimensions as well as trace fins on the copper side, concluding that the additional trace fins and larger PCB area increase the capabilities of both current and thermal properties. Adding additional components to traces to improve the current and thermal capabilities was also found by (Drumea & Marghescu, 2021) experimentation using step increases of the current methodology on traces with additional tinning or soldering copper wires to the trace showed that the additional material on the trace improved the capabilities of the trace, as shown in

Figure 2.1, indicating that the addition of vias has the potential to improve the capabilities of the traces consequently improving the circuits reliability.

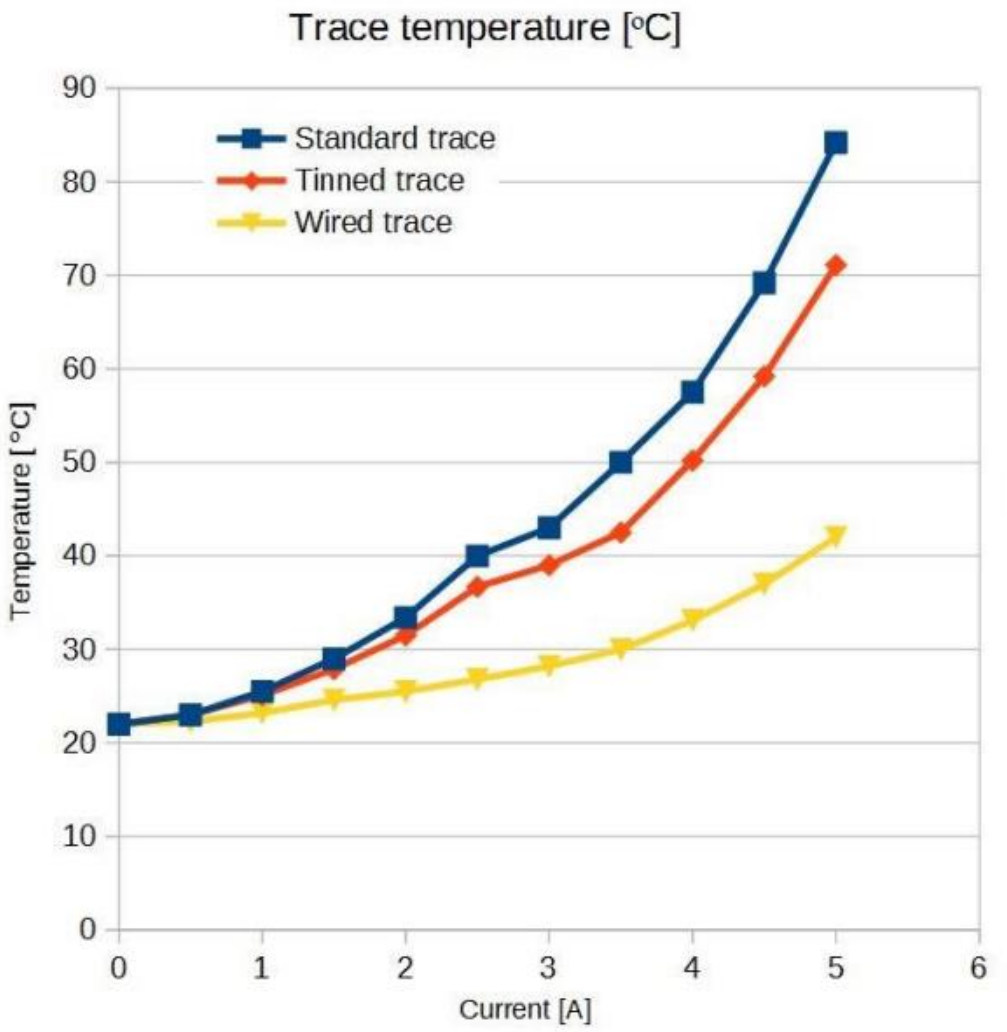

Figure 2.1: Temperature profiles of different types of 1 mm width PCB traces at different test currents (Drumea & Marghescu, 2021).

An alternative area to investigate the capabilities of traces is through reliability experimentation, such as the investigation conducted by (Elliot & Brown, 2023), which had a more direct focus on comparing different trace bend angles, utilising a similar methodology to (Drumea & Marghescu, 2021) to find the maximum current of a straight, 45 and 90 degree angles traces, concluding no major difference between the three. While the angles do not pertain to this research, the results (Elliot & Brown, 2023) for the maximum currents, as shown in Table 2.1:, indicate that overcurrent experimentation can be conducted with low power

supplies, giving the project feasibility to conduct reliability experimentation utilising non-specialised power supply.

Table 2.1: Results of the maximum current on straight traces, traces with 45° bends and traces with 90° bends (Elliot & Brown, 2023).

	Straight Traces	Traces with 45° bends	Traces with 90° bends
Number of samples	28	60 (4 PCBs x 15 traces)	60 (4 PCBs x 15 traces)
Mean maximal current	2.773 A	2.823 A	2.842 A
Median maximal current	2.773 A	2.831 A	2.904 A
Standard deviation	0.120 A	0.270 A	0.207 A

While (Elliot & Brown, 2023) also conducted thermal imaging of the traces upon failure; the methodology was limited as it was done based on interest compared to analysis; it showed that at the location of the failure, the temperature exceeded the maximum temperature threshold of the FLIR thermal camera utilised at 270 ℃, which identifies the requirement to have a thermal camera with a higher maximum temperature than 270 ℃, or to adjust the methodology to accommodate the limitation.

2.3.2 PCB Via Current Capabilities

Vias have an important role in PCB design of routing electrical signals through the layers of a PCB; when it comes to the current carrying capabilities, the vias are typically not alone and are integrated with traces, pads, and components; even so, there has been limited research into via current properties alone. The analysis carried out by (Reeves et al., 2002) looked at the influence via liner had on the resistance and current density; it was found that the liner would focus the current along the liner sidewall and would concentrate at the base of the liner when transferring to the trace; the research also showed that the resistance would increase as the current density increased. The resistance increases due to the current density increasing was also found by (Zhao et al., 2012) research into Direct Current (DC) in chip-scale Through Silicon Via (TSV) in ICs using a power simulator; similarly, the research also found that the current density crowds at the point where the wire connects to the via, as shown in Figure 2.2 (b) and (c), the crowding was more concentrated in a smaller area.

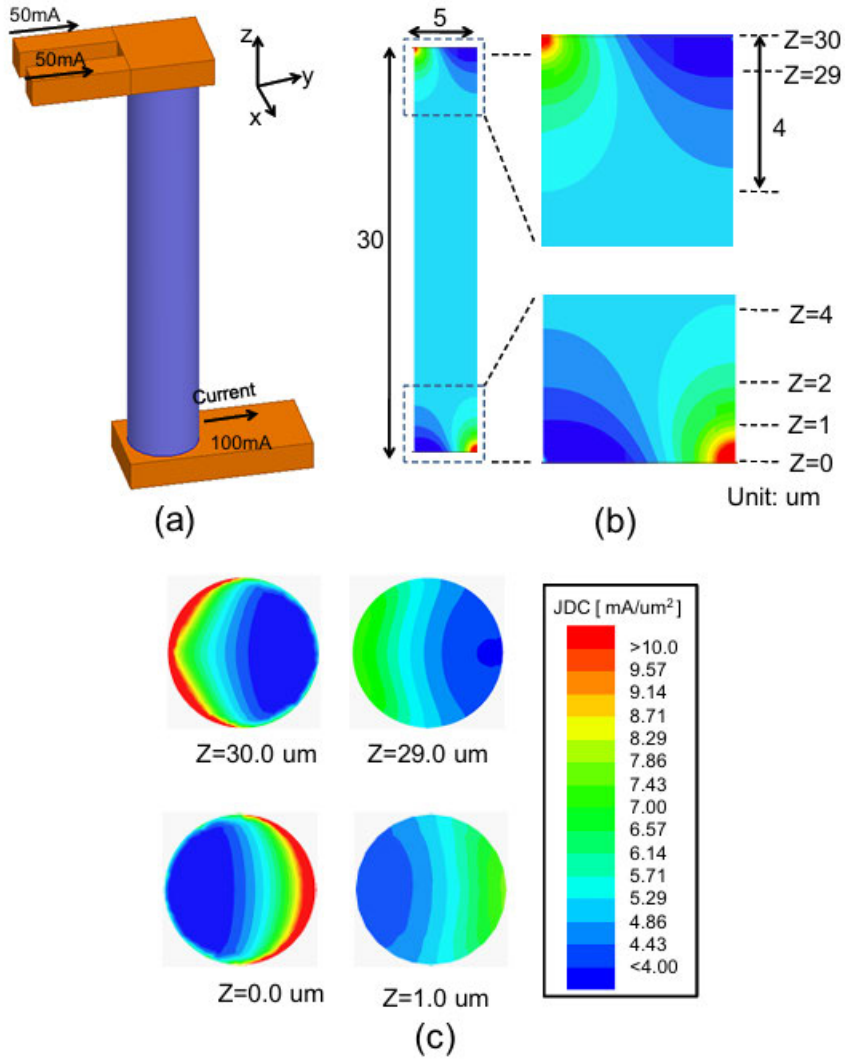

Figure 2.2: The test case of a TSV and power wires with current crowding. (a) showing 3D model of the via and wires with the direction of current, (b) ZY(side view) plane current density distribution, and (c) XY (top-down) plane view for Z=30.0 µm, 29.0 µm, 1.0 µm and 0.0 µm (Zhao et al., 2012).

The impact of the connections between the wire, cable, and trace with the via was also identified by (Müller et al., 2010) as the location non-uniform current arises from high-frequency systems, (Müller et al., 2010) also identified the non-uniform current based on the proximity of the vias to each other based on two vias. This proximity is due to vias producing an electric field around them based on the current density and is also confirmed by the research conducted by (Zhao et al., 2015), which, through simulation with only two vias (Power and Ground (GND)), concluded that that the current density was more concentrated when the vias were in closer proximity to each other as shown in Figure 2.3.

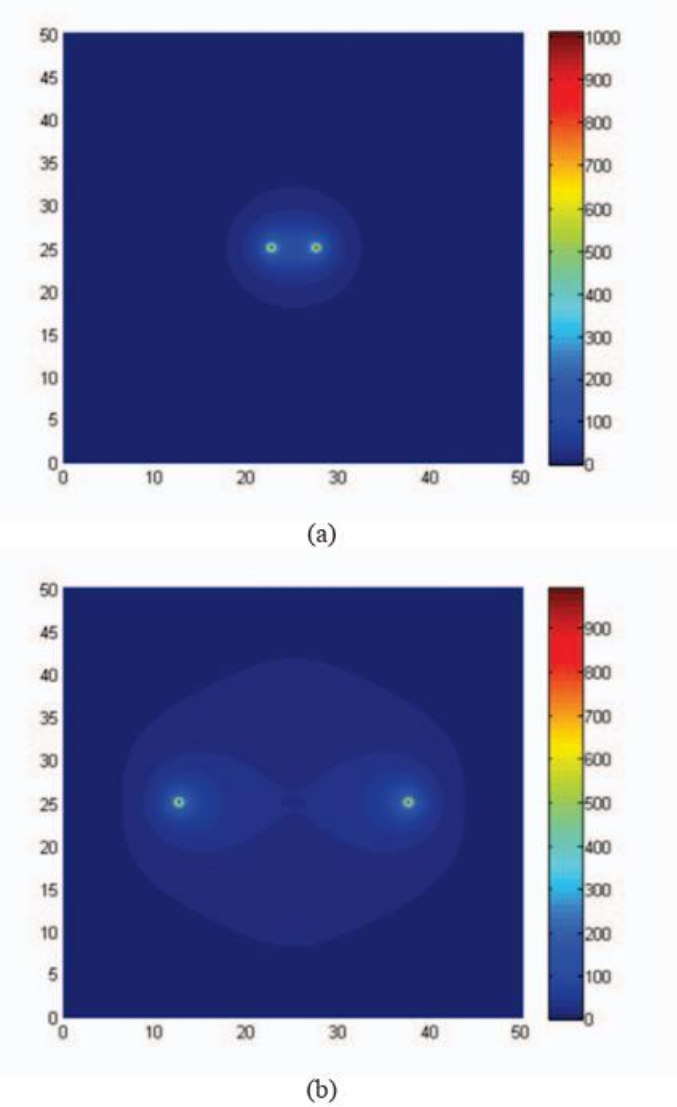

Figure 2.3: Current density plot with different distances (a) 5mm, (b)25mm (Zhao et al., 2015).

While looking at different types of vias compared to the project, the findings by (Müller et al., 2010; Reeves et al., 2002; Zhao et al., 2012) demonstrate that the area of greatest impact for current is the transition zone between the via and interconnections which would predictably be the area that leads to failure. Further, the findings by (Müller et al., 2010; Zhao et al., 2015) indicate that the proximity of the vias will impact the surrounding circuits; as only two vias, there is room for further investigation into the impact of a larger quantity of vias.

2.3.3 PCB Via and FR-4 Thermal Capabilities

As PCB boards are designed with a greater density of components, thermal considerations are increasingly required in the design stage of PCBs to compensate for heat generated by the

components due to Jouile's law (Equation 1.2) power losses, components are typically linked to a heatsink; this can be achieved through thermal vias or pads. (Shen et al., 2018) developed a model for the optimisation of PCB vias thermal resistance for this purpose, concluding that to achieve minimum thermal resistance, there is an optimal via diameter. The model was further expanded upon by (Shen et al., 2020) to include the thermal resistance of PCB pads designed for surface mount components; the model design showed that the dimension impacted the thermal properties of the pads; the larger the radius, the more it dissipated the temperature. This function of vias and pads dissipating the temperature may indicate a beneficial function in a circuit, and an increased quantity could dissipate more heat.

The ability of vias to dissipate heat will have an impact on their surroundings, such as traces, components and the dielectric; the research by (Beng et al., 2013) utilising FloEFD 11 software to simulate the impact of two types of thermal vias, PTH and copper filled have on the surrounding FR-4 dielectric, found the quantity and configuration had an impact on the thermal resistance. (Beng et al., 2013) found that the increased number of vias will reduce the thermal resistivity of the FR-4 dielectric, which will allow the FR-4 dielectric to readily transfer more heat, as shown in Figure 2.4and Figure 2.5; it was also found that there was an optimal amount of vias at 19 before the impact was negligible, as shown in Figure 2.5.

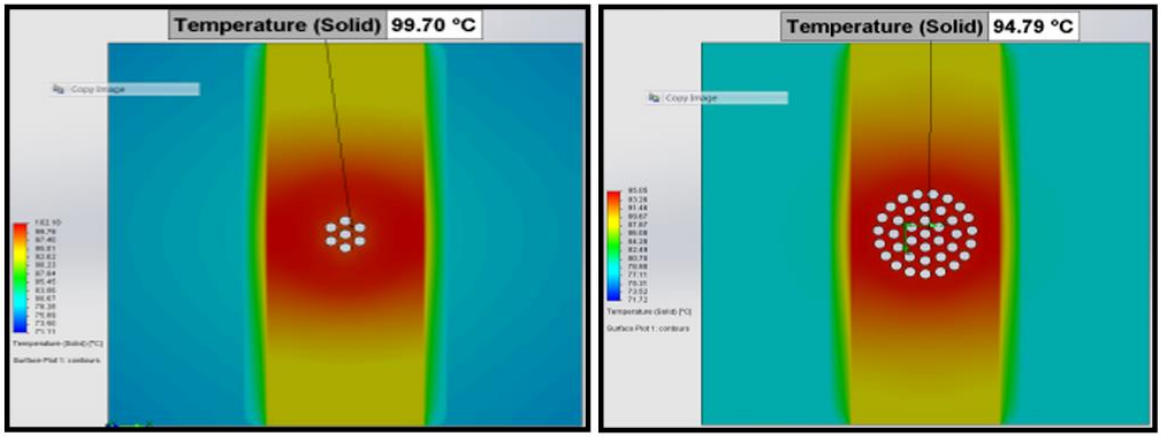

Figure 2.4: Thermal images of the temperature distribution on FR-4 PCB with different quantities of vias (Beng et al., 2013).

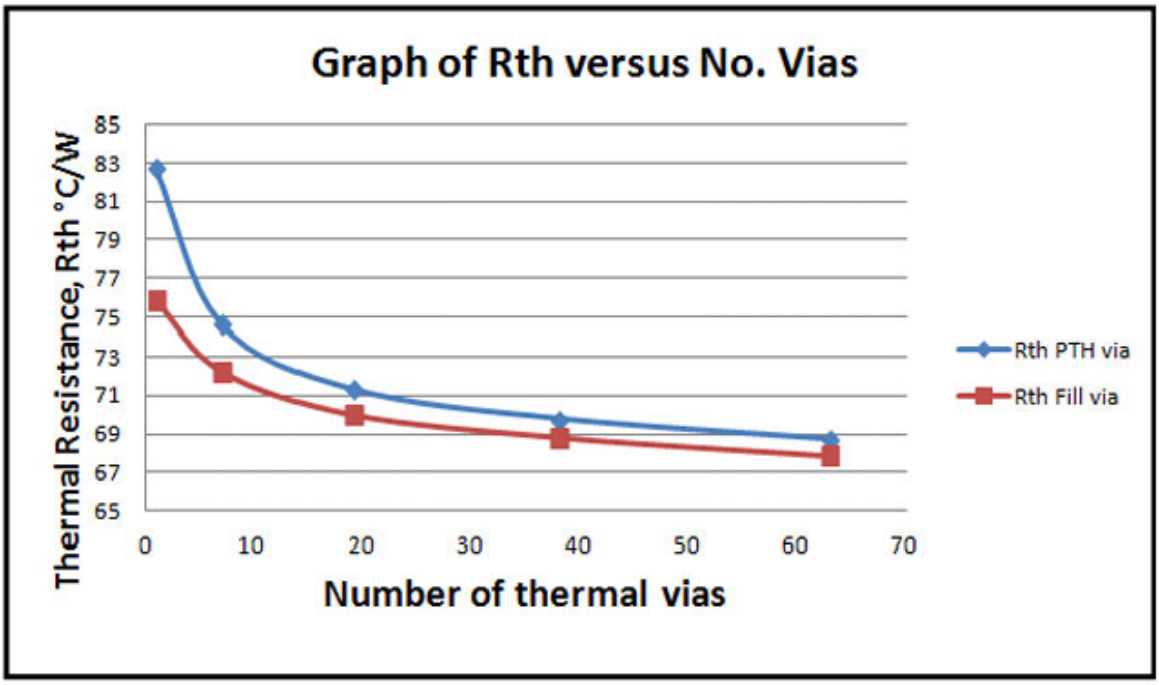

Figure 2.5: Graph of the thermal resistance of the FR-4 PCB compared to the number of vias (Beng et al., 2013).

The dielectric that holds the circuits is just as important as the circuit itself; while it does not directly carry current, it can be impacted by the heat produced by a current-carrying component. (Polanský et al., 2014) Utilising a thermal ageing technique, a study was conducted on the thermal endurance of PCB FR-4 epoxy laminate. Utilising microscopy and thermal analyses (Polanský et al., 2014) found that the longer the FR4 is exposed to high temperatures, the rate of decomposition was more profound on the FR-4 dielectric, with the internal structure showing inert pyrolytic decompositions and having reduced oxygen diffusion at the surface-air interface. These findings by (Polanský et al., 2014) focus on the aging process compared to a rapid increase in temperature or temperature going above 200℃, which the project PCBs will encounter.

2.3.4 Combined PCB Trace and Vias

The literature on PCB interconnections has focused on the individual interconnections even within the same research, such as the investigation by (Coppola et al., 2008) looking at the current density limits of traces, one via and five vias, all separately while also investigating the thermal properties of both interconnections types. To investigate the trace's current carrying capability (Coppola et al., 2008), applied three phases of Alternative Current (AC) to three

traces concurrently at 140 A until failure; the traces would be either alone or connected to components, while the via investigation consisted of the step increases of the current until failure on its own dedicated PCB as shown in Figure 2.6 (a) and (c).

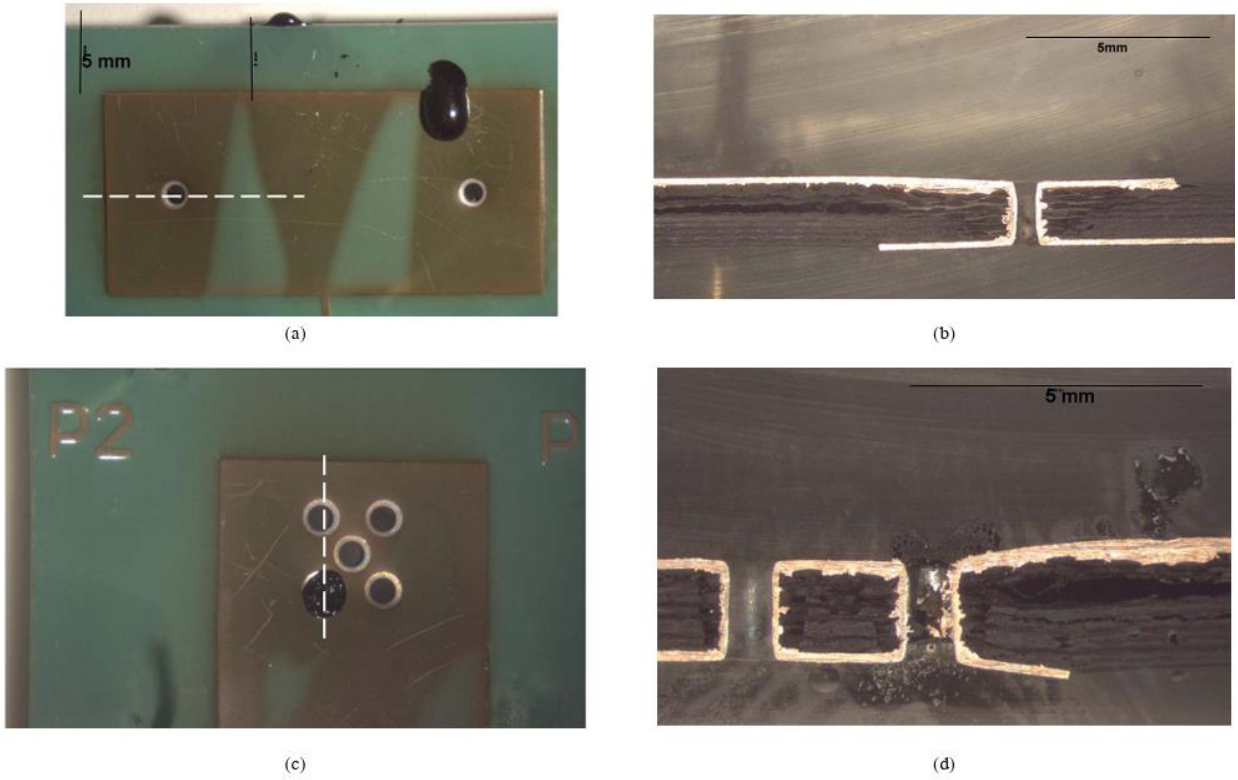

Figure 2.6: Images of the maximum current testing of vias conducted in (Coppola et al., 2008), (a) layout of the single via testing after testing, (b) cross-section view of the FR-4 for a single via, (c) layout of the five via grouping after testing and (d) cross-section view of the FR-4 for five via grouping.

One finding from the experiment related to the quantity of vias from (Coppola et al., 2008), is that when a failure occurred for the five via compared to the one via, the five via had a greater maximum current at 90 A compared to 70 A for the single via hole at lower temperatures, 250-280 °C compared to 300-350 °C respectively, this difference is illustrated in Figure 2.7. (Coppola et al., 2008) concluded that the deciding mechanism of failure in the research was the softening point of the FR-4 dielectric, as can be seen in Figures 2.5 (b) and (d) unless components were attached, which then changed the limiting factor to the components. More specifically (Coppola et al., 2008) identified with the vias, the additional limiting factor for the single via was the via itself compared to the five via, where it was the trace connected to the plate.

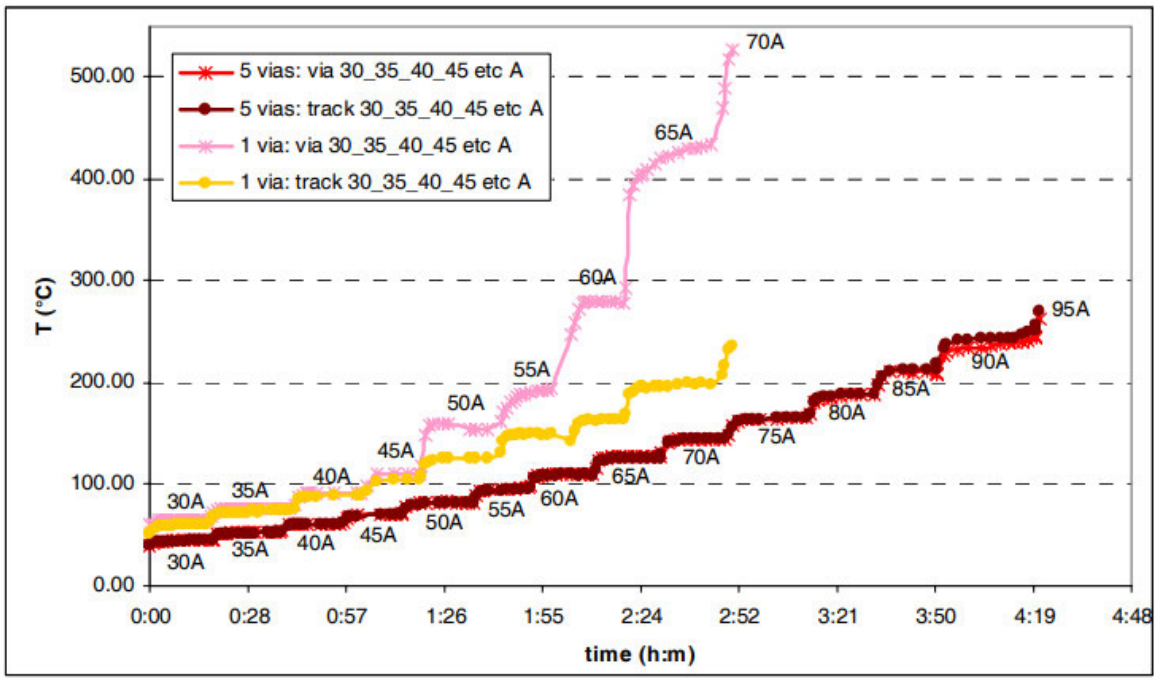

Figure 2.7: Temperature profile of trace and via in the case of single via hole and multiple via hole (Coppola et al., 2008).

The literature presented by (Coppola et al., 2008) has some key differences to this project, the first being that the maximum current methodology for the trace and vias were separate and different, compared to the project where both are part of the same circuit utilising the same methodology. The second is the configuration of multiple vias shown in Figure 2.6(c); the vias are shown to be in an x-shape grouping, while the projects will have them in series interconnected with traces and not placed on conductive plates as shown in Figure 2.6(a).

2.4 IPC Standards

In any manufacturing industry, to maintain consistent design, manufacturing, and safety processes, it is necessary to use standards; in the PCB industry, Association Connecting Electronics Industries® (IPC), an international organisation, sets the standards for PCB design, with the previous standard, IPC-2221, being the industry standard in regards to maximum current. (Adam, 2004) investigated the equations set out for IPC and DN in the IPC-2221 for trace maximum current and compared it to experimental data in preparations for the next iteration of standards, IPC-2152. (Adam, 2004) found that the equations set out in the IPC-2221 for trace maximum current were only relevant to specific specifications of the trace, only being effective to boards with a 35 µm copper layer on the back with a long copper trace of 35

μm. This review helped shape the development of the IPC-2152 standard, which had equations associated with multiple parameters of traces for maximum current. The IPC-2152 standard was reviewed by (Bunea et al., 2010), who also compared the equations laid out in the standard to experimentations, concluding there is a significant difference between the experimental results and the IPC, stating the IPC maximum current is lower due to their focus on the safety of the trace. (Bunea et al., 2010) demonstrate that the maximum current of a trace with copper foils of thickness of 35 μm will be far different than what is calculated using Equation 2.1.

$$I = 0.028 * \Delta T^{0.46} * W^{0.76} * t^{0.54} \quad (2.1)$$

Where: I is the current (A);
ΔT is the temperature difference between the trace and environment (°C or K);
W is the Trace width (mil);
t is the Trace thickness (mil).

2.5 PCB Reliability

As PCBs become denser with components, there is an increase in the potential for faults, reducing the reliability of the PCBs; there has been academic literature that identifies and categorises failure in PCBs. Physical reliability starts at the manufacturing stage with (Sankar et al., 2022) conducting a review of PCBs coming from manufacturing and identifying 34 defects ranging from soldering defects to damaged PCBs and breaking them down into categories. A failure can occur at any stage in the lifespan of a PCB, (Slee et al., 2009) conducted an investigation into the multiple failure types and categorised them into an introduction to the PCB research paper. The investigation by (Slee et al., 2009) identified some key failures that relate to the project, the first being power losses caused by Joule's law (Equation 1.2), where the currents will cause the resistive element (trace, vias, pad) to generate enough heat to cause damage to the surrounding areas, which can lead to insulation breakdown, including the dielectric of the PCB. The second is the contamination of the circuits. (Slee et al., 2009) address that dirt, dust, or soot can create shorted resistive paths that lead to failure. (Slee et al., 2009) also identified that groupings of vias can generate electric fields, as shown in Figure 2.8, that can lead to localised insulation breakdown, which further confirms what was found by (Beng et al., 2013; Müller et al., 2010; Zhao et al., 2015).

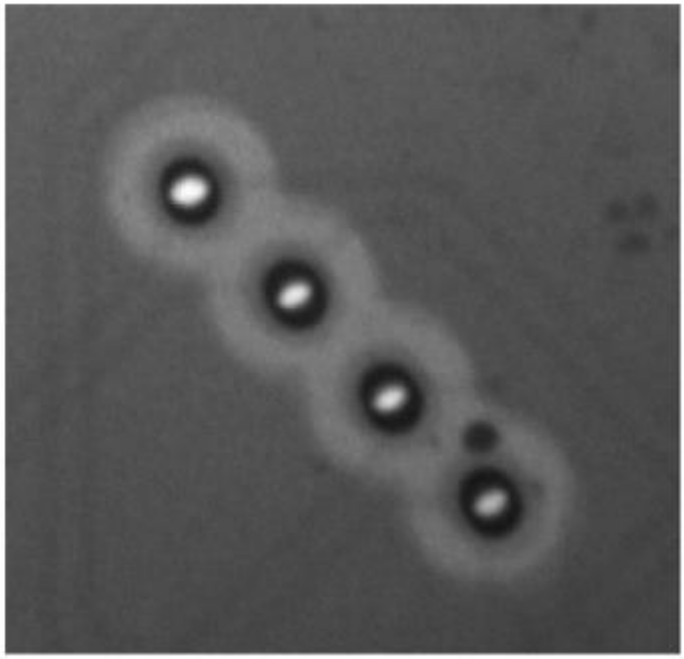

Figure 2.8: Via field (Slee et al., 2009).

A lot of the faults identified in the literature have a common theme of being caused by current; this is also noted by (Ji et al., 2010) in more specific research on copper-plated blind vias, noting that overcurrent would cause coarsened copper grains led to a decrease in the ductility of the plating layer, which can cause the via to crack, Identifying the method that a via can fail during overcurrent testing.

The literature reviewed is based on reliability and influences the methodology of the project by identifying the need for inspection upon receiving manufactured PCB based on (Sankar et al., 2022) and requires cleaning based on (Slee et al., 2009). The literature also identifies the importance of reliability in PCBs with the number of ways it can fail and gives importance to conducting reliability experimentation.

2.6 Conclusion

The literature presented in this review has demonstrated there is a knowledge gap with the PCB design rule via minimisation and its relation to reliability in terms of interconnection circuits and demonstrated the feasibility of meeting the dissertation objectives:

- Conduct research on the impacts vias have on a PCB circuit.
- Conduct to-failure experimentation through over-current on PCB circuits with different quantities of vias to determine the maximum current, thermal and physical properties of the circuits.
- Analysis of the data collected from the experimentation to determine the impact the quantity of vias has on the reliability of the circuits
- Conduct a comparison between the analysed data based on the quantity of vias to determine if there is a noticeable difference between the circuits.
- Conclude if the quantity of vias either is detrimental to the reliability of PCB circuits validating the design rule of via minimisation or is beneficial to the reliability of PCB circuits invalidating the design rule.
- Provide recommendations in PCB design by using vias based on the results.

The literature has also influenced the methodology of using a step increase of current that was used in (Coppola et al., 2008; Drumea & Marghescu, 2021; Elliot & Brown, 2023) with a starting point determined based on Equation 2.1 from the IPC-2152 standards and modified for the specific circuits.

Chapter 3

Methodology

3.1 Introduction

This dissertation aims *to investigate the design rule of via minimization in PCB manufacturing by observing the impacts that the quantity of vias has on the reliability of PCB circuits;* to meet this aim, one of the objectives of the project was to conduct to-failure experimentation through over-current on PCB circuits with different quantities of vias to determine the maximum current, thermal and physical properties of the circuits. To meet this objective, the methodology was broken into two stages: the initial preparations, which include:

- Administration.
- PCB Design.
- PCB pre-experiment checks.
- Experiment Setup.
- Preliminary maximum current experimentation.
- Preliminary thermal experimentation.

The initial preparations were required to conduct the second stage, which was to conduct statistical analysis through experimentation through the following experiments and investigation:

- Maximum current experiment.
- Thermal experiment.
- Physical properties investigation

Through the statistical analysis, a conclusion will be drawn as to whether the quantity of vias impacts the reliability of a PCB circuit. The methodology closes with a critical review and conclusion.

3.2 Administration

The first stages of the project were to conduct the administrative tasks involved in conducting the project effectively, accurately, and safely; this involved acquiring the test equipment, accessing the industry standards, and conducting a risk management plan.

3.2.1 Test Equipment

To conduct both the maximum current and thermal experiments, several test equipment were required, with several being acquired before the project started. The equipment acquired previously is the Jesverty SPS-3010N DC power supply displayed in Figure 3.1, the UT61E+ multimeter in Figure 3.2, the Protech InfraRed Thermometer displayed in Figure 3.3 as well as the computers used to store and process the data, which are all used in both tests; the final equipment needed was a thermal camera for the thermal testing. In the months of March, contact was made with the technical staff at the University of Southern Queensland (UniSQ) Springfield campus to inform them of the need to gain access to a thermal camera, this would be followed up the week after the flexible learning period of trimester one to acquire access to a thermal camera for thermal testing to be conducted during the inter-period between trimester one and two. One week before the end of trimester one, the FLIR i5 infrared thermal camera, as shown in Figure 3.4 was acquired to conduct the thermal testing for the project over a two-month period, with it being inspected after a month to ensure the equipment was in good condition. The key parameters of the test equipment can be found in Table E1 (see **Appendix E**).

The primary parameters of the Jesverty SPS-3010N DC power supply in Figure 3.1 that are relevant for this dissertation are: it has a 0 – 30 V range and a 0 – 10 A range which can be found in Table E1 and in (Jesverty, n.d.).

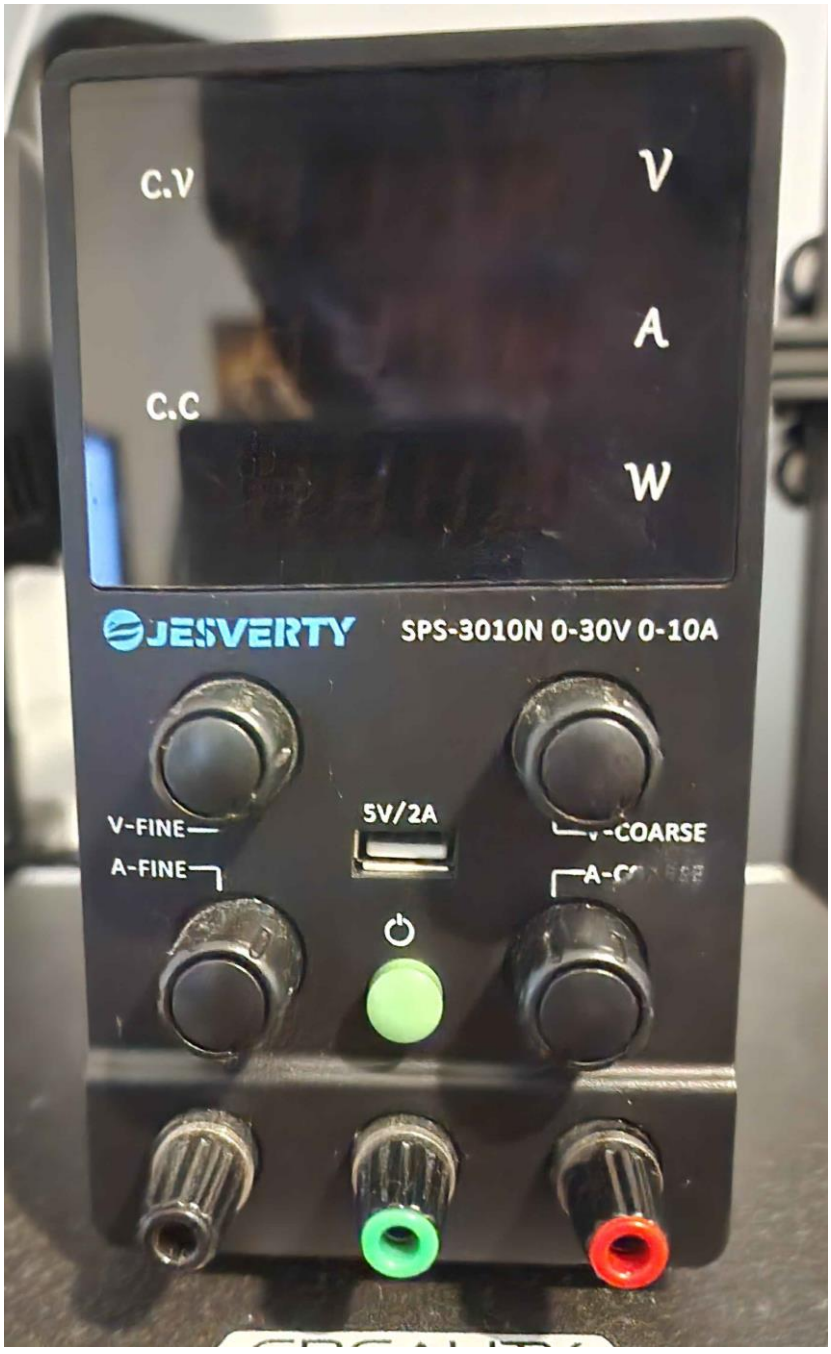

Figure 3.1: Jesverty SPS-3010N DC power supply.

The primary parameters of the UT61E+ multimeter displayed in Figure 3.2 that are relevant to this dissertation are it has a maximum current of 20 A, with a 10 A, 240 V overload protection built into the multimeter; the multimeter can also be connected to a computer or laptop through a Universal Serial Bus (USB) to record electrical readings, these detail can be found in Table E1 and in (UNI-T, n.d.).

Figure 3.2: UT61E+ multimeter.

The Protech infrared thermometer a shown in Figure 3.3 has a thermal measuring range of -50 °C to 500 °C which is the primary parameter to impact this dissertation, the information can be found in Table E1 and (Protech, n.d.).

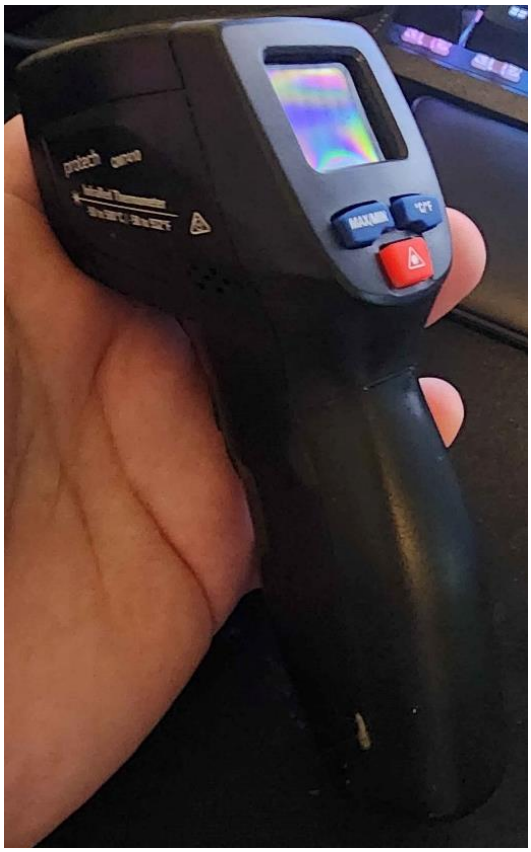

Figure 3.3: Protech infrared thermometer.

The Flir i5 acquired from UniSQ has a maximum temperature of +270 °C, and it captures the images in infrared; the maximum temperature is a limitation for this dissertation; the details can be found in both Table E1 and (FLIR, 2011).

Figure 3.4: Flir i5 infrared thermal camera.

3.2.2 Industry Standards

To conduct experiments on PCB circuits, it was deemed optimal to use the industry standards for PCB design and manufacturing, IPC 2221, “Generic Standard on Printed Board Design” and IPC 2512, “Standard for Determining Current Carrying Capacity in Printed Board Design”, as these were identified in the literature review (IPC, 2003, 2009) . As these are international standards, they could not be accessed through the UniSQ standard database, and the library staff had to be contacted by the supervisor; the library staff investigated access to these standards, but it was found that the access may not even be granted and if it were, it would be limited to one person to access it with heavy restrictions based on the investigation by the library staff. The experiment methodology was built based on the methods found in the literature review that included methods from IPC 2221, such as (Elliot & Brown, 2023) or similar experiments, such as those conducted by (Coppola et al., 2008).

3.2.3 Risk Assessment

As the project involves testing with live power and meeting the objectives, the following risks were identified and assessed:

- Electrocution.
- Fire and burns.
- Sharp Cuts.
- Chemicals due to fumes.
- Chemical due to cleaning agent.
- Ergonomics due to repetitive movements.

After the assessment of the number of risks, a risk management plan was constructed in Figure C1-C14 (See. **Appendix C**) using SAFETRAK to reduce the risk to acceptable levels using the hierarchy of safety controls for conducting testing at UniSQ Springfield engineering build (F Block) and personal residence. The management plan was then forwarded and approved by the project supervisor (See. **Appendix C**).

The risk assessment was conducted for the UniSQ Springfield Engineering Building (F Block) as there was the potential of requiring testing to be conducted at the university; this was a precaution and was not used in the testing.

3.3 PCB Design

To conduct testing for the impact on the reliability due to the quantity of vias, three types of circuits were designed using EasyEDA software, and twenty of the same circuits were manufactured on two-layered PCBs. The three types of circuits were similar in design; all three had two through-hole pads for external connection points and traces interconnecting between the pads and vias. The key difference was the quantity of vias on each type of circuit; the quantities are one, five and ten vias. The one via circuit is for reference circuit as it is the minimum number of vias a circuit can have; the five and ten via circuits the vias are placed in series. The dimensions of the circuits are presented in Table 3.1, and each different circuit can be seen in Figure 3.5-3.7, with (a) showing the layout of the circuits, (b) showing the top layer of a circuit, and (c) showing the bottom layer of a circuit.

Table 3.1: Parameters of the PCBs and circuits on the PCBs.

Parameter	Value	Parameter	Value
Substrate	FR-4 TG130	Trace width	0.305 mm (12.0 mil)
Board thickness	1.6 mm	Via Inside Diameter	0.3 mm (11.8 mil)
Board size	100 mm x 100 mm	Via Outside Diameter	0.5 mm (19.7 mil)
Number of circuits per Board	20	Pad shape (dimension)	Rectangle (1.524 mm x 1.524 mm)
Number of copper layers	2 (Top and bottom)	Pad hole (dimension)	Round (0.914 mm diameter)
Trace thickness	35 µm (1 oz or 1.37795 mil)	Hole Plating thickness	18 µm
Trace length from via to pad (one via)	13.988 mm	Trace length from via to pad (five vias)	10.988 mm
Trace length from via to pad (ten vias)	7.488 mm	Trace length in between vias (five and ten vias)	1 mm
Total trace length (one vias)	27.976 mm	Total trace length (five vias)	25.976 mm
Total trace length (ten vias)	23.976 mm		

The dimensions of the circuits and PCB were based on commonly used values that were both cost and time-efficient in manufacturing; due to this consideration, the choice was to work with two-layer FR-4 PCBs. The next design consideration was the circuits on the PCBs; based on the work done by (Elliot & Brown, 2023), it found that traces required a high current to break the circuit, and with the focus on the vias for this dissertation, the vias would have to be the minimum common dimension available; for a two-layered PCB the inner dimension was limited to 0.3 mm, which limited the outer dimension to 0.5 mm. the limitation on the vias also impacted the limitation on the trace, for the traces the width was to be as close to the inner dimension as possible without being below it, this limited it to a width of 0.305 mm. The dimensions of the pads were for the interconnection to external testing equipment, and the deciding factor was the pad hole dimension; this allowed enough room for header pins to be inserted.

The length between the centre of the pad holes was 30 mm; this was to maximise the number of circuits on the PCB for manufacturing, with each PCB having a total of 20 circuits per board. The manufacturing was done by JLCPCB, which also manages the EasyEDA software used in this project. The PCBs were manufactured with different colours; the circuit with one via was green, as shown in Figure 3.5; the PCBs with five vias circuits were yellow, as shown in Figure 3.6; and the PCBs with ten via circuits were manufactured in red, as shown in Figure 3.7, this was to make the circuits easy to identified throughout the project.

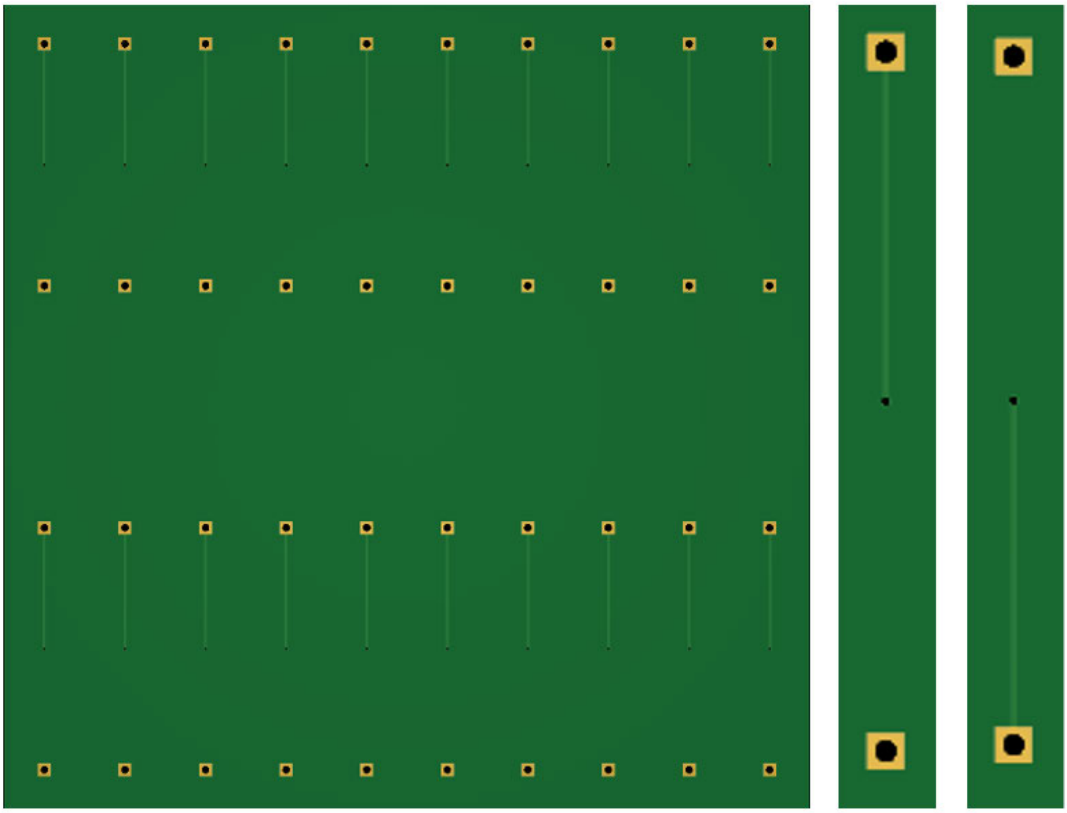

Figure 3.5: PCB Design for experimentation with one via on a circuit, (a) the PCB with two rows of ten testing circuits, (b) the top layer view of a single circuit, (c) the bottom layer view of a single circuit.

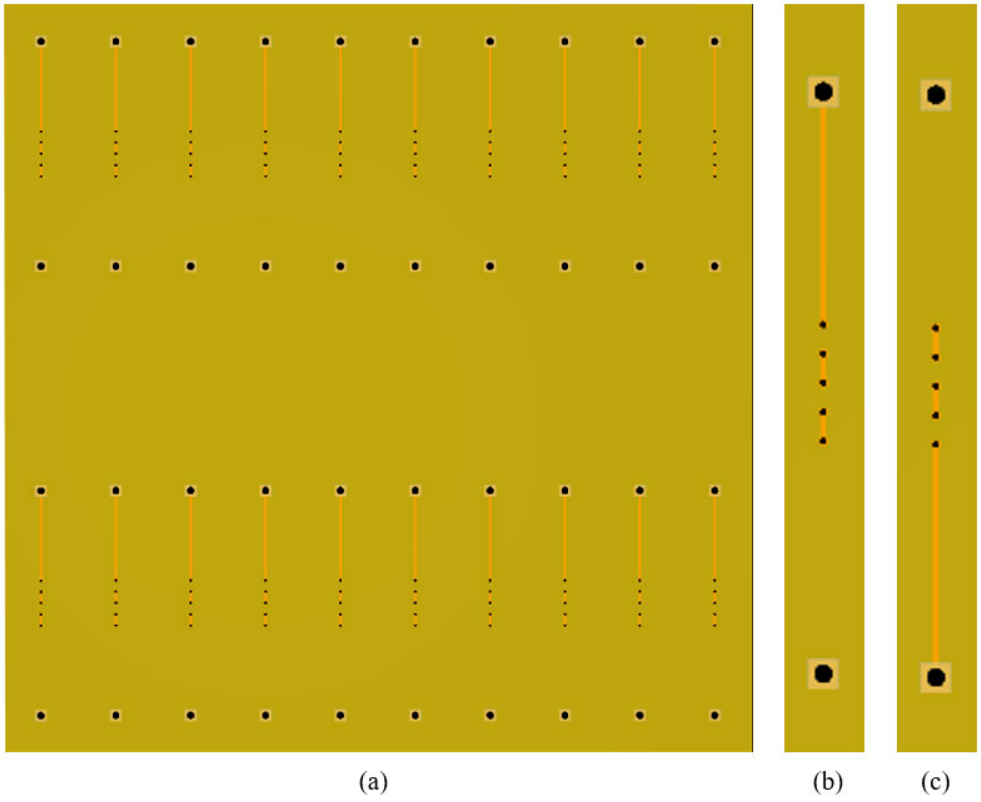

Figure 3.6: PCB Design for experimentation with five vias on a circuit, (a) the PCB with two rows of ten testing circuits, (b) the top layer view of a single circuit and (c) the bottom layer view of a single circuit.

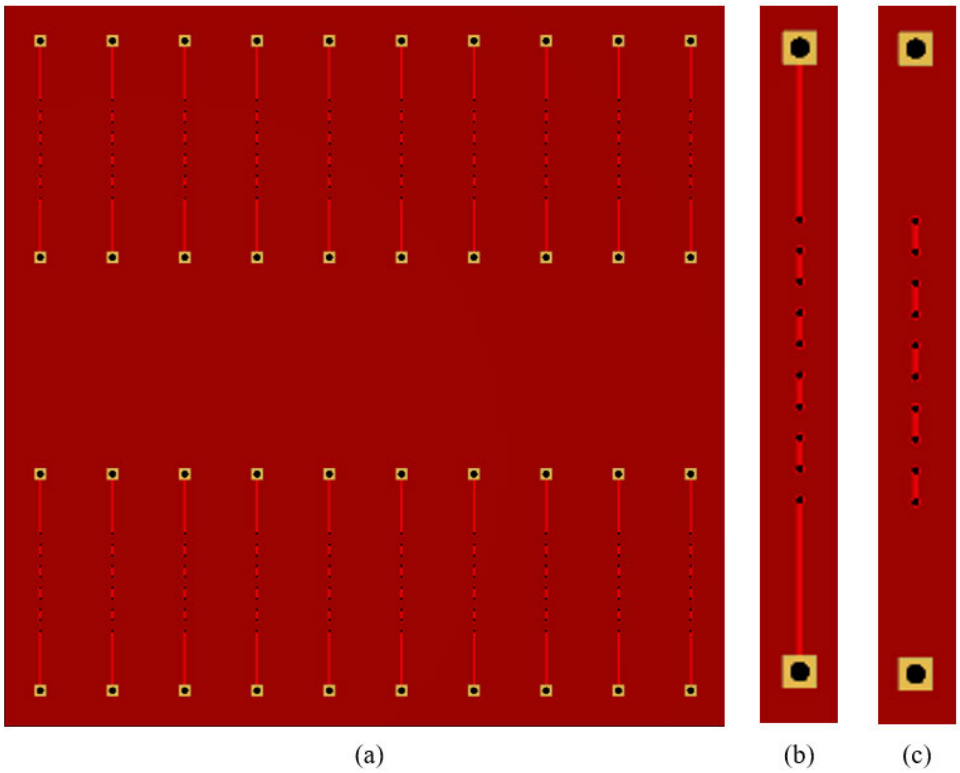

Figure 3.7: PCB Design for experiment with ten vias on a circuit, (a) the PCB with two rows of ten testing circuits, (b) the top layer view of a single circuit, (c) the bottom layer view of a single circuit.

3.4 PCB Pre-Experiment Checks

Upon receiving the PCBs, each circuit was inspected using eyesight and a magnifying glass for any damages that could impact the testing; if any noticeable circuit had damage, they were marked not to be used during the testing. After inspection, the PCBs were all cleaned using Isopropyl Alcohol (IPA) and a clean cloth to remove any manufacturing/transportation debris, dust or contaminates. Following the cleaning, using a permanent marker, each card was labelled for easy identification, as shown in Figure 3.8; the naming convention is as follows:

Vx-y-z1

Where: x is the quantity of vias;
y is the card number;
z indicates which experiment, C for maximum current and T for thermal.

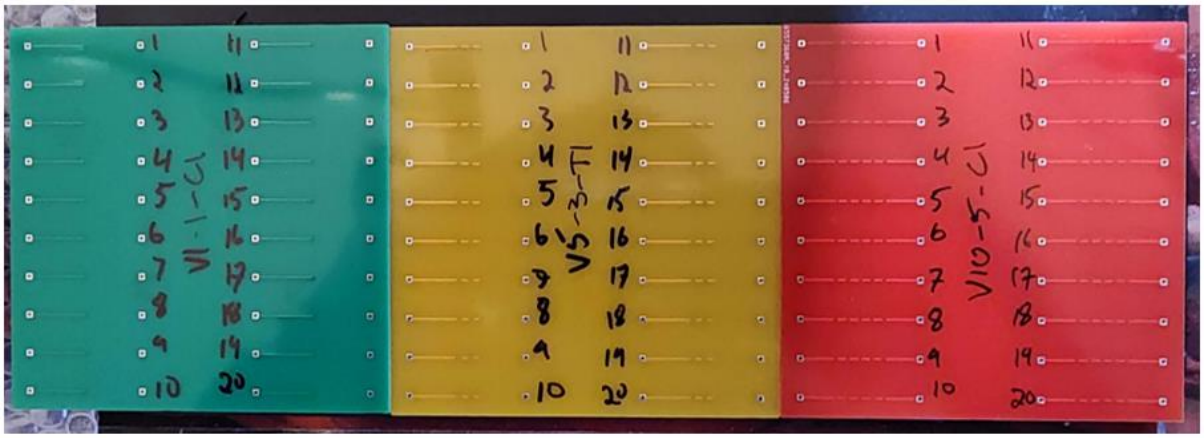

Figure 3.8: Photo of three PCBs with the three different circuits, (a) one via circuits for maximum current experiment, (b) five via circuits for thermal experiment and (c) ten via circuits for maximum current experiment.

A separate PCB for both maximum current and thermal testing of each type of circuit was labelled as spare in the card number position on the label; these were prepared for when a test would unexpectedly fail, data was not recorded, or the test was interrupted due to outside influence. Following the labelling of PCBs, each circuit would be labelled 1 through to 20 to be easily identifiable through video and photo, and for the organisation of data collected, the exception was the preliminary testing circuits, as these were labelled t1 to t10. Following the labelling of the PCBs, 110 circuits' resistance was measured using the UT61E+ multimeter to compare the mean of the resistance between the one, five and ten via circuits, then the cards would be stored in 23 ± 1.5 °C room at below 50% humidity until required for testing. Only 110 circuits were measured because the resistance measurements were decided upon after several circuits had already been tested and had reached failure; 35 circuits were tested of the one via circuits in the maximum current experiment and 5 for the thermal experiment to maintain consistency between circuits the same circuit numbers were missed on the other two circuit types.

3.5 Experimental Setup

To investigate the impact on the reliability due to the quantity of vias, the test will require a set-up utilising the test equipment and allowing current to flow through the PCB circuits; the set-up will be the same for both the maximum current and thermal testing. The power will come from a Jesverty DC power supply, with a maximum of 30 V and 10 A. The positive lead will

connect directly to the UT61E+ multimeter, which is connected to the circuit being tested on the PCB through alligator clips with header pins; the multimeter is required to be in the circuit to measure current(Jesverty, n.d.; UNI-T, n.d.). The circuit being tested is connected to a bank of three parallel high-power resistors (3.3 Ω, 100W) through alligator clips using a header pin; the resistors are placed in parallel to split the current between them based on KCL and to reduce the overall power consumption by each resistor, the resistors are then connected to the return on the power supply (ARCOL, 2008). This schematic of the experimental setup is shown in Figure 3.9.

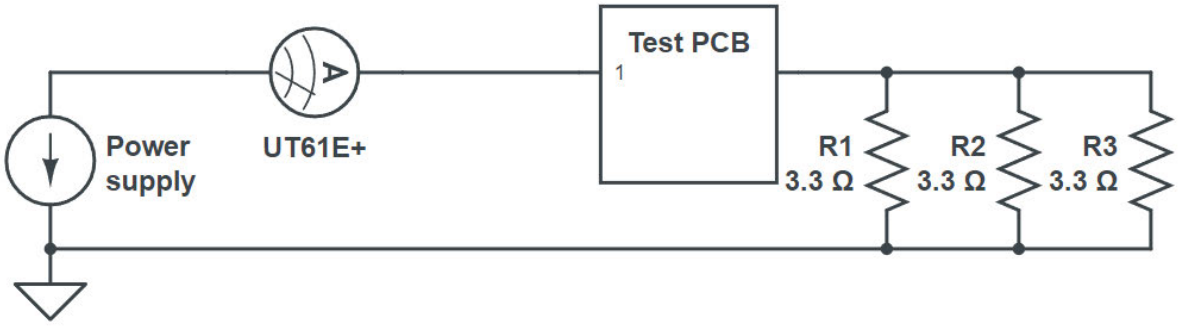

Figure 3.9: Schematic of the experimental set-up for testing the PCB circuits.

The setup also includes an extraction fan with a carbon filter to remove the fumes that the burning FR-4 dielectric produces and is placed just behind the PCB; the PCB is also held aloft by helping hands soldering station, which has a ring light with a magnifying glass to help with lighting when it comes to photos/videos being recorded. The final addition to the set-up is a camera holder positioned to hold the Samsung Galaxy S22 ultra above the experiment for both photos and videos of the testing, all shown in Figure 3.10. The UT61E+ is connected to either a PC or laptop through USB to record the current value using the UT61E+ recording software; the software was set to take sample readings every 1000ms, and this reading was used as the source of the timing involved in the experiments as it was consistent in all experiments. The parameters and details of the equipment used can be found in Table E1 (See **Appendix E**).

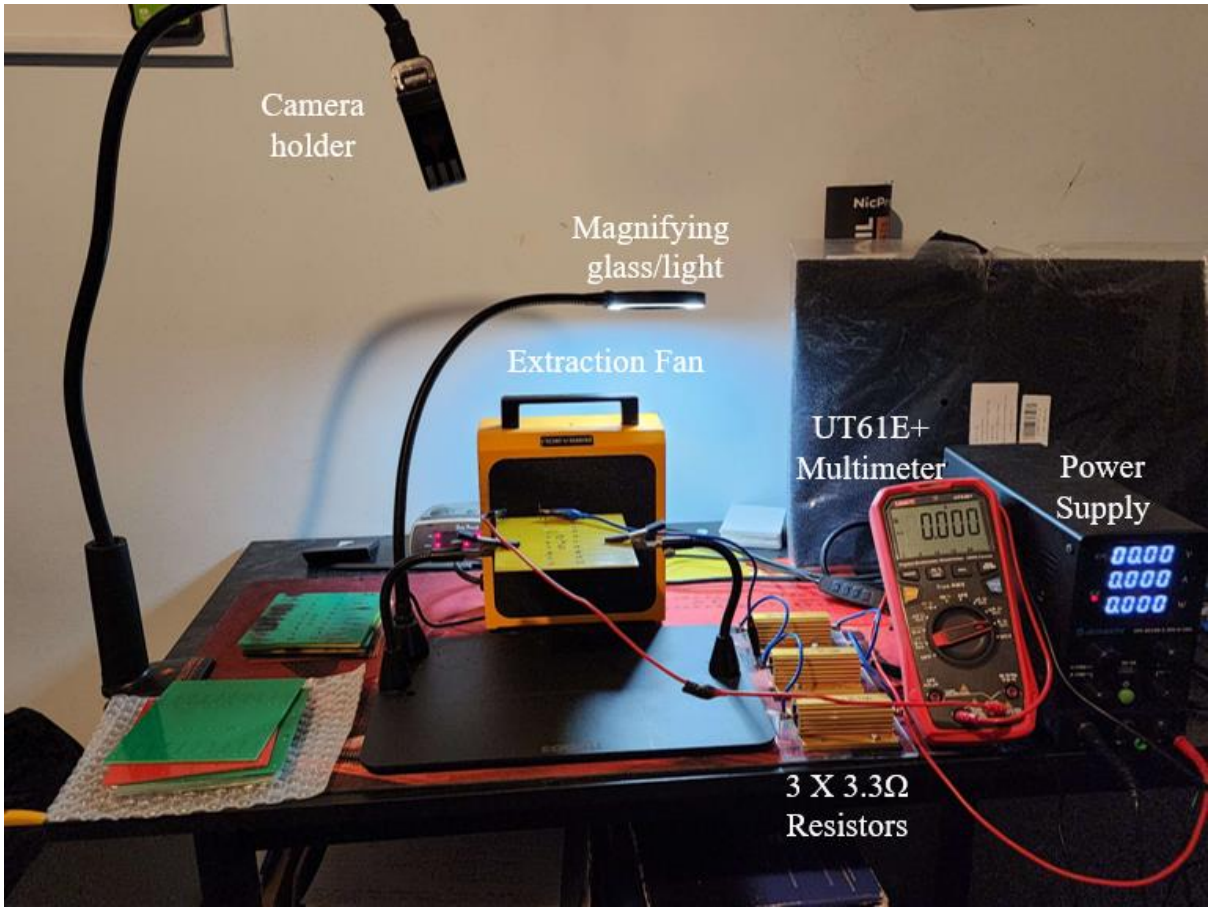

Figure 3.10: The experimental set-up for both maximum current and thermal testing, image displaying, the camera holder for the Samsung 22+ ultra, the magnifying glass/light, the extraction fan, power supply, parallel resistors, the UT61E+ multimeter and a PCB in a ready testing position.

3.6 Dissertation Experiments

The experiments address the overall aim of the dissertation *to investigate the design rule of via minimization in PCB manufacturing by observing the impacts that the quantity of vias has on the reliability of PCB circuits* and meet the objective to conduct to-failure experimentation through over-current on PCB circuits with different quantities of vias to determine the maximum current, thermal and physical properties of the circuits. The experiments were split into two focus areas, maximum current and thermal experiments, with both also addressing the physical properties. Splitting the experiments was decided upon due to requiring the FLIR i5 thermal camera for the thermal properties; when it was time to start experimentation, it was unknown if a thermal camera was able to be acquired, what time frame this acquiring would occur and how long the thermal camera would be available for experimentation. So to ensure

that there were results that could be analysed for the dissertation was to start with experimentation that had a focus on maximum current and then to conduct a second experimentation that would have a more focused approach to the thermal properties. Both experiments would undergo preliminary experimentation to decide upon the optimal methodology for gathering the required data for analyses and to meet the objectives and aim of the dissertation.

3.6.1 Preliminary Maximum Current Experimentation

Upon the delivery of the PCBs and after approval of the risk management assessment, preliminary experimentation was conducted on up to ten circuits of each quantity via circuits; these were designated as testing circuits, and no official data was recorded. The purpose of these experiments was to:

- Ensure the circuits can fail.
- Practice using the test equipment.
- To decide on a methodology for testing

All three purposes were tested simultaneously; multiple methods were tested due to the limitations of not having direct access to the industry standards (IPC, 2003, 2009) and relying on previous literature. The first method was to increase the current at set values, 50 mA, 100 mA or 200 mA, at steady rates over set times of 5 seconds or 10 seconds starting at 500 mA; it was found that these methods were difficult to replicate consistently in consecutive tests and were not used. The 500 mA starting current was chosen as it falls below the maximum current calculated from Equation 2.1, as was identified from (Bunea et al., 2010) from the IPC2152 standard (IPC, 2009), which was calculated to be 634.6 mA based on a temperature rise of 10 ℃ from an ambient temperature of 23 ℃ , trace width 0.305 mm (12.0 mil) and thickness 35 μm (1 oz or 1.37795 mil) from Table 3.1, the maximum is well below the actual failure point of the trace, as the maximum current equation (Equation 2.1) in the IPC standards is for safety over reliability.

The next method tested was to start at higher current values, 4 A and 5 A; while this allowed for faster experiments, it was decided it was more appropriate to start at lower values to capture the full range of the current and to start at a value that fell below the maximum based on Equation 2.1. The third method tested was to increase the current at set intervals and pause for a set time before increasing to the next level. The current increases tested were 50 mA, 100 mA

or 200 mA with 5 seconds or 10 seconds pauses with the starting current at 500 mA; this proved the most consistent method to replicate between experiments and was the main method used in the experiment. It was decided to use 100 mA steps, 50 mA was too small to be accurate with a manual dial on the power supply, and 200 mA was too large for any accuracy and to use the 5-second pause as with the range of current values this allowed for more expedited experimentation.

During the preliminary testing, the equipment required was also tested. The first area was to ensure the multimeter, and its associated software could record the information required and how to convert the information into Excel files for future analysis. The next test equipment that required further understanding and testing was the Jesverty SPS-3010N power supply; during the testing, it was found that it was optimal to set the power supply voltage to maximum and increase the current throughout the testing; this would prevent the need to increase the voltage at any stage throughout the experiment, it was also identified that due to using mechanical dials there was potential for the dial to slip and cause far greater increase of the current than desired and fallback plans were developed in the experimentation.

The final check was to ensure the circuits all failed, as the work conducted by (Elliot & Brown, 2023) identified that traces required high current values to fail, and designing the traces' width to be just larger than the inner diameter of the vias, the trace width was greatly increased in comparison and posed the possibility that the circuits may not fail, the test showed that all circuits could fail with the limit of 10 A of the power supply.

3.6.2 Maximum Current Experiment

To conduct experimentation to find the maximum current of a circuit based on the quantity of vias, the starting point is the PCB that is being tested, which is inspected one final time for any defects, and the circuits are cleaned using IPA. Once the PCB is cleaned, it is attached to the set-up, as shown in Figure 3.10, with the positive lead(red) on the left side of the circuit and the negative lead (blue) on the right side. Once the PCB has been added to the circuit, it is inspected to ensure the set-up is complete. Then, the PCB temperature is measured by a Protech infrared thermometer, and the starting temperature of the PCB needs to be at 23 ± 1.5 °C. The starting current is set to 500 mA; once the current was at 500 mA, the experiment was held at this value for 15 minutes to precondition the circuit as outlined by (Elliot & Brown, 2023).

Once the circuit had been preconditioned for 15 minutes, the current was increased by 100 mA every 5 seconds until the circuit failed or reached the power supply's maximum current (10 A). If a circuit reached the maximum current of the Jesverty DC power supply, the current would be held for 5 seconds and then would be dropped just below 10 A as the UT61E+ multimeter has a maximum threshold of 10 A before overload protection initiatives, which cut off its readings after a minute, the time held near maximum current would be recorded for comparison between the different quantities of vias. Once a circuit had failed, the PCB was allowed to cool to the ambient temperature of 23 ± 1.5 °C and cleaned using IPA; testing was conducted on the adjacent circuit.

To find out if the quantity of vias impacts the maximum current of the circuit, the data collected using UT61E+ recording software is saved as a .csv file, which Excel uses; the file is then converted to a .xlsx file to be able to save Excel functions used. To find the maximum current at failure, the Excel function max() is used; the value found is then recorded in a separate calculations Excel file for statistical analysis of all circuits tested. To compare the maximum current between the quantity of vias of each circuit, the mean (Equation 3.1), median (Equation 3.2) and standard deviation (Equation 3.3) are calculated from all the maximum currents recorded from each quantity of vias one, five and ten using the Excel functions AVERAGE(), MEDIAN() and STDEV.S() respectively; these values are tabularized, and a box plot is produced to show the spread of maximum current based on the quantity of vias on the circuits.

$$\bar{x} = \frac{\sum_{i=1}^{n} x_i}{n} \tag{3.1}$$

$$Median = \left(\frac{n+1}{2}\right)^{th} \tag{3.2}$$

$$s = \sqrt{\frac{\sum(x_i - \bar{x})}{n-1}} \tag{3.3}$$

Where: $\bar{x}$ is the mean of the set x_i values;
x_i is the data points;
n is the total number of data points;
s is the standard deviation.

3.6.3 Preliminary Thermal Experimentation

The Preliminary thermal experiments were conducted at the end of trimester one, once the FLIR i5 thermal camera was acquired from the technical staff of UniSQ; the purpose of the preliminary was to:

- Practice and understand the capabilities of the FLIR i5.
- To decide on a methodology for the thermal experiment.

The first purpose was to understand how the FLIR i5 works and what the optimal way to use the camera was to get the required data to be analysed to address the main objective of the project. The second purpose was to determine a method that was optimal and time-efficient in gathering the required thermal data for statistical analysis, as it was undetermined how long access to the FLIR i5 thermal camera was for the student.

The methodology was going to be like the maximum current experiment modified to account for thermal measurements; the first modification that was tested was to extend the step times from five seconds to ten, twenty or thirty seconds to allow time for the temperature to settle and time to capture the images, through testing it was decided that the 20-second pause was optimal, it allowed time for the temperature to settle and time for thermal and physical photos to be taken. The second modification that was tested was the time for the preconditioning, as the previous preconditioning time was based on the current; the time that was tested was ten minutes, five minutes and one minute, through testing it was found that both the temperature and current would settle in five minutes and this was what was used in the experimentation.

The third modification was to change the starting value, as with the maximum current, it was decided to get the full range of current as the focus was on the current; for this experiment, it was decided to start at a higher current level, based on the maximum current it was seen that around the 4 A to 6 A range there was no noticeable difference in the PCB and circuit based on thermal heat, so testing was conducted on 4 A, 4.5 A,5 A, 5.5 A. After testing, it was decided to go with a 5 A starting current; this value was low enough that any change caused by thermal properties did not occur for several current levels above for any of the three circuits.

3.6.4 Thermal Experiment

From the preliminary thermal experimentation, the method used to investigate the thermal impacts on the reliability of PCB circuits based on the quantity of vias is a modified maximum current experiment method. Like the maximum current, the PCB and circuits being tested were

cleaned using IPA and physically inspected for defects before being placed in the experiment set-up and cables connected to the circuit. Once the test PCB was in the experimental set-up and the PCB temperature was at 23 ± 1.5 ℃ the current would be increased to 5 A, as it was shown in the previous experiment that the thermal impacts on the circuits did not occur until a minimum of 7 A was applied, so it was decided to start far lower, once at 5 A the circuit would be held at this current for 5 min for preconditioning this allowed time for the temperature to settle at this current. Once the preconditioning period of t minutes had finished, the current was increased by 500 mA every 20 seconds until the circuit failed, or if the circuit met the maximum current (≈ 10 A) of the power supply, the current would be reduced to just below 10 A to avoid the UT61E+ multimeter overload protection until the circuit failed. Once a circuit failed, the power was reduced to 0 current, and the PCB was allowed time to cool to ambient temperature (23 ± 1.5 ℃) and cleaned using IPA; testing was conducted on the adjacent circuit.

To collect the relevant data for the statistical analysis of thermal impacts on the circuits, a thermal image using the FLIR i5 and a physical image using the Samsung Galaxy 22 Ultra were taken at each 500 mA stage starting at 5 A. The images produced by the FLIR i5 had three temperature values, as shown in Figure 3.11. The top left is the temperature of the crosshair location, and the bottom two numbers represent the minimum and maximum temperatures in the range of colours the camera can detect, with the limitation of +270 °C (FLIR, 2011). For the statistical analysis, the highest temperature value was added to the calculations Exile file to find the mean (Equation 3.2), median (Equation 3.3) and standard deviation (Equation (3.4) at each current 500 mA level for each type of the three circuits tested, which is tabled; also, the means of card tested of each circuit type was plotted, the table and plot allow for a compare and contrast of the thermal data collected. Further analysis is conducted through the images taken; the thermal images are compared between the circuits to observe how the thermal pattern changes based on the quantity of vias and where the concentration of the heat is radiating from to get a further understanding of how the temperature reduces the reliability of the circuits. Similarly, the physical images will be compared at each current level to observe how the PCB and circuit break down based on the thermal properties.

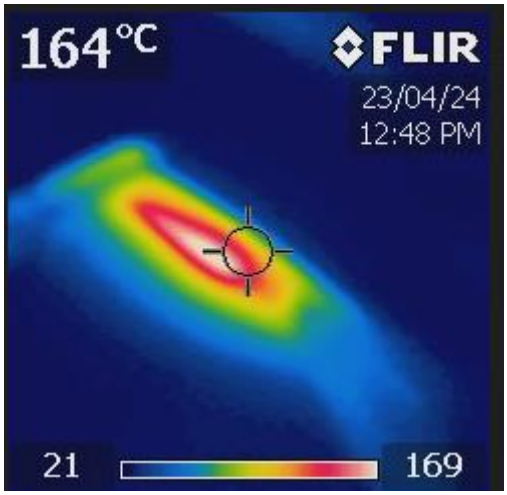

Figure 3.11: Thermal image of a five via circuit during practice attempts at using the FLIR i5 infrared thermal camera.

3.6.5 Physical Properties Investigation

Throughout the Maximum current and thermal experimentation to further investigate the impacts the quantity of vias has on the reliability of the PCB circuits, the physical properties of the PCB and circuit will be investigated in the following three areas:

- Failure location.
- Physical changes towards failure.
- Area of destruction caused by failure.

3.6.5.1 Failure location

While the Maximum current testing was being conducted, utilising a camera stand to hold a Samsung Galaxy 22 Ultra above the set-up, as shown in Figure 3.10, to record the test while the current was being increased; this video was watched after the testing to observe where the failure occurred; this would also be followed up by a physical inspection utilising ether eyesight or a magnifying glass to confirm the failure location, or if the failure happens on the bottom layer where the video was not recorded.

For the circuits tested through the thermal experiments, the photos of failure or just after that were produced using the Samsung Galaxy 22 Ultra were inspected alongside physical inspections utilising eyesight and magnifying glasses to identify the location of failure that occurred on the circuit. The following locations were decided to be the most likely locations for failure to occur:

- Trace
- Via
- Pad
- FR-4 Dielectric

Two additional categories were added to the list; these include the no-failure, as there was a potential for circuits to not fail during testing. The other category was undetermined for when the failure occurred; due to the destructive nature of the failure and limited viewing angles, it could not determine the failure point on the circuit; this usually could happen when a failure occurred on the bottom layer where the video could not be recorded, or physically observed.

3.6.5.2 Physical changes towards failure

For the physical changes towards failure, the photos of the circuits at each current level that were produced by the Samsung Galaxy 22 Ultra during the thermal experiment were compared between the three circuit types of one, five and ten vias, this comparison is to see if the changes in the physical properties are impacted based on the quantity of vias. Physical changes include colour changes in the dielectric or circuit, melting or burning of material, fumes or flames produced while the current changes, at the point of failure or after failure.

3.6.5.3 Area of damage due to failure

When a circuit or component on a PCB fails, it can cause undesired destruction in an area that can impact other circuits or components. To investigate further the physical properties that are impacted by the quantity of vias, a photo was taken of each PCB by the Samsung Galaxy 22 Ultra after all circuits on the PCB had been tested; for both the top and bottom layers of the PCB, these photos of the damaged area will be compared between each type of circuit, one, five and ten vias to determine if the quantity of vias impacted the area of damage. Furthermore, an estimate of the damaged area will be calculated; the area will be calculated based on three shape types:

- Rectangle (a) in Figure 3.12
- Ellipse (b) in Figure 3.12
- Tear-shape (c) in Figure 3.12

These shapes were chosen as the damage area closely resembles these shapes which will contain errors in the calculations; for the rectangle, Equation 3.4 will be used; for the ellipse,

Equation 3.5 will be used; and for the tear-shape Equation 3.6 will be used, Equation 3.6 is a combination of the area of a triangle with a semi-circle.

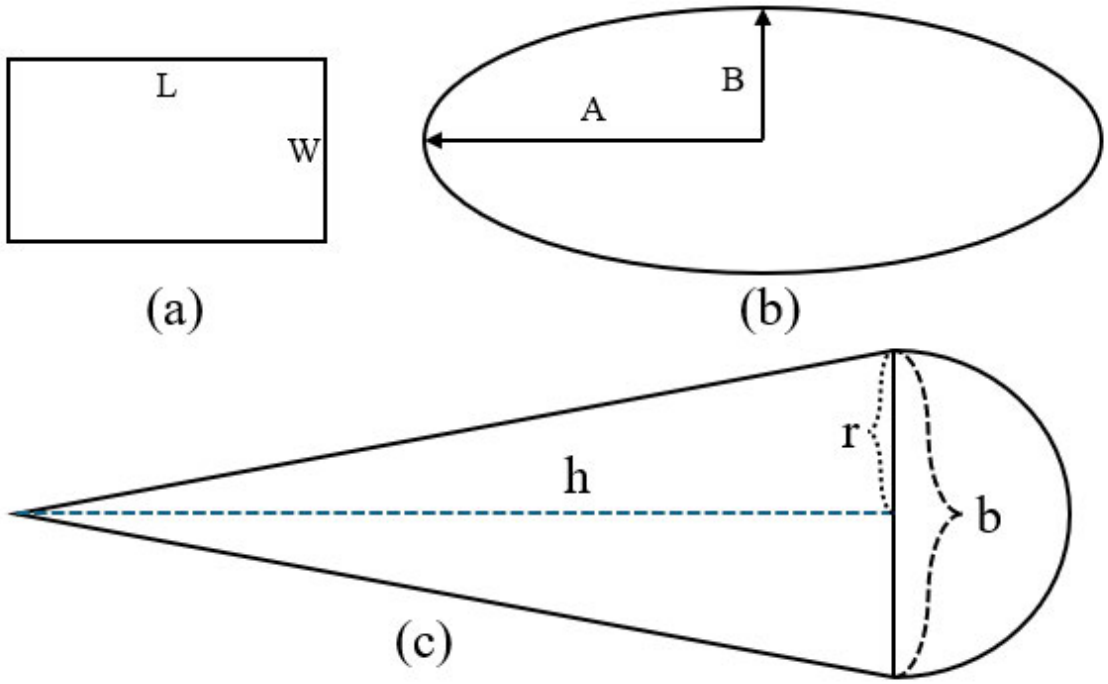

Figure 3.12: The shapes and dimensions used to determine the area of damage after failure are (a) rectangle, (b) ellipse and (c) tear-shape.

$$A_{rectangle} = L * W \tag{3.4}$$

Where: $A_{rectangle}$ is the area of a rectangle (m^2)

L is the length of the rectangle (m)

W is the width of the rectangle (m)

$$A_{ellipse} = \pi * B * A \tag{3.5}$$

Where: $A_{ellipse}$ is the area of an ellipse (m^2);

B is the semi-minor axis of an ellipse (m);

A is the semi-major axis of an ellipse (m)

$$A_{Teardrop} = \frac{1}{2}\pi r^2 + \frac{1}{2}bh \quad (3.6)$$

Where: $A_{Teardrop}$ is the area of a teardrop (m^2)

r is the radius of a circle (m)

b is the base of a triangle (m)

h is the height of a triangle (m)

The damaged area of all circuits that underwent both the maximum current and thermal experiment will be measured in two sections: the widest part of the damaged area and the length of the damage along the circuit; this will then be used in the equation best reflected by the shape. The area will be calculated into three sections: the top layer area, the bottom layer area and the total area in Excel; the mean (Equation 3.1), median (Equation 3.2) and standard deviation (Equation 3.3) will then be calculated of each area section, then tabularized to be compared between the three types of circuits in the experiments.

3.7 Critical Review of the Methodology

With the methodology being implemented and results collected, there are several areas of the methodology that were not optimal in the approach to meeting the objective: to conduct to-failure experimentation through over-current on PCB circuits with different quantities of vias to determine the maximum current, thermal and physical properties of the circuits.

One essential part of the methodology that was not optimal was the lack of access to industry standards, specifically IPC 2221, “Generic Standard on Printed Board Design”, and IPC 2512, “Standard for Determining Current Carrying Capacity in Printed Board Design”, as either of these standards have industry methodology on how to test and compare the maximum current and thermal properties of PCB interconnections such as the trace or via as was observed in (Elliot & Brown, 2023). Furthermore, the standards also had another benefit; they potentially contain testing methodology around measuring both the maximum current and thermal properties together in a single experiment. In this dissertation, due to unknown timing impacts associated with the FLIR i5 thermal camera, these experiments were separated to ensure there were results to be analysed; ideally, these experiments would be combined and would follow methods laid out in industry standards, as this allows the result to be compared more directly, and more circuits would be tested adding more to the statistical analysis.

The circuits that were used in the dissertation were also not the most optimal, particularly the ten via circuit; this is due to the quantity of vias on the circuit. The ten via circuit had an even number of vias which changed the physical pattern of the circuit; the one and five via both have on both the top and bottom layer a trace that goes between the pads and the vias; in comparison, the ten via has both traces on the same layer. The optimal approach would be to have the quantity of vias as either all even or odd, so the circuit pattern is the same between the circuits

Regarding the equipment, the one area limiting the dissertation was the thermal camera FLIR i5 and its limitation of a maximum reading of +270 °C for the temperature, limiting the results that can be achieved from the experiments. This would allow a better comparison of temperature at set current levels and compare the maximum temperature of the circuits. Another limitation was the number of cameras used in the thermal experiment, as it was found, especially in the five via circuits, failure could occur on the bottom layer, limiting the impact the top layer images or video had in determining the physical properties at failure. In future experiments associated with this dissertation or associated research area, the use of thermal cameras with greater maximum temperature would be the optimal approach and the use of multiple cameras, both thermal and photographic, to capture both the top and bottom layer properties at the stages to failure and at the point of failure.

Regarding analysis and comparison of the results of the experiments, one area was the process of calculating the damaged area of the circuits; the methodology used with based shapes has produced results that lack accuracy and are only effective because the difference between the area values was significant. If the results were closer in values, this methodology would not be sufficient in conducting an effective comparison to determine the impacts the quantity of vias have on PCB circuits regarding physical failure.

3.8 Conclusion

After conducting the experimentation, obtaining results, and identifying non-optimal approaches in the methodology through critical review, the methodology used in this dissertation still effectively obtained results that met the following objective:

- Conduct to-failure experimentation through over-current on PCB circuits with different quantities of vias to determine the maximum current, thermal and physical properties of the circuits.

This Objective was used to meet the other objectives and address the overall aim of the dissertation *to investigate the design rule of via minimization in PCB manufacturing by observing the impacts that the quantity of vias has on the reliability of PCB circuits*.

Chapter 4

Results and Discussions

4.1 Introduction

The main aim of the dissertation is *to investigate the design rule of via minimization in PCB manufacturing by observing the impacts that the quantity of vias has on the reliability of PCB circuits.* In Chapter 4, Results, the data collected from the methodology is analysed to meet two of the objectives to address the main aim of the dissertation. The objectives are to analyse the data collected from the experimentation to determine the impact the quantity of vias has on the reliability of the circuits and to conduct a comparison between the analysed data based on the quantity of vias to determine if there is a noticeable difference between the circuits. This chapter is broken into the following key sections:

- Resistance
- Maximum current
- Thermal properties
- Comparison between the maximum current and thermal properties results
- Physical properties of failure

Each of these sections will cover the results produced from the methodology and then will be analysed to address the aim and objectives of this dissertation.

4.2 Resistance of the PCB Circuits

4.2.1 Results

Table 4.1 shows the statistical analysis of the 110 circuit resistances that were measured, demonstrating a difference between each type of circuit. The resistance increased by 0.01 Ω for every five via circuits for the mean and median values. Table 4.1 also shows the calculated series resistance of the traces with the vias of each circuit type using Equation 4.1 and the information presented in Table 3.1 in the previous chapter, with the assumption that the copper plating has the same resistivity as the trace at 1.724×10^{-8} Ωm (Moaveni, 2019). The result of

the calculations show a similar increase in resistance as the measured circuits, but at a reduced increase of approximately 0.005 Ω compared to 0.01 Ω; this minor discrepancy can be explained by multiple factors, such as material purity, the plate or trace dimension are not exactly the values presented in Table 3.1, inconsistencies in the manufacturing process and measurement errors through the multimeter. This overall increase in the resistance of the circuits based on the number of vias will impact the power loss due to heat due to Joule's law based on Equation 1.2.

Table 4.1: Results of the resistance measurement of the three types of circuits.

	One Via	**Five Via**	**Ten Via**
Number of samples	110	110	110
Mean resistance measured	0.233 Ω	0.242 Ω	0.252 Ω
Median resistance measured	0.230 Ω	0.240 Ω	0.250 Ω
Standard deviation	0.015 Ω	0.021 Ω	0.015 Ω
Calculated resistance of both the trace and via	0.0468 Ω	0.0505 Ω	0.0559 Ω

$$R = \rho \frac{L}{A} \tag{4.1}$$

Where: R is the resistance in (Ω);
ρ is the resistivity of the material (Ωm);
L is the length of the conductor (m);
A is the cross-sectional area of the conductor (m^2)

4.2.2 Resistance of the PCB Circuit Summary

As the current in a circuit depends on the resistance based upon Ohm's law and the current will impact the power losses experienced based upon Joule's laws (Equation 2.1), this difference in the resistance will impact the overall performance of the circuits and the reliability of the PCBs.

4.3 Maximum Current

4.3.1 Results

The first experiment to be completed was the maximum current, Table 4.2 showing the numerical statistical results of the experiment. The one via circuits was the control of the experiment, and the results show that it has a mean current of 8.53 A and a close median of 8.44 A; the difference of 0.09 indicates there are few outliers in the maximum current result, with a standard deviation of 0.37 A, indicating most of the values were close to the mean of 8.53 A. Furthermore, Table 4.2 shows that the maximum current of five via circuits improved compared to the one via circuits, the mean improved by 130 mA to 8.66 A and the median 197 mA to 8.64 A, with the median and mean being near equal it demonstrates there are next to no outliers with the five via circuits, with the standard deviation is also increase by 734 mA, to 0.45 A indicating the maximum current values are further away from the mean when compared to the one via circuit.

Additionally, Table 4.2 shows the maximum current of the ten via circuits. When the maximum current of the ten via circuits is compared to the five via and one via circuits, the average and median maximum currents are lower. Compared to the five via circuits, the ten via circuits current is lower by 436.7 mA for the mean and 482.5 mA for the median and compared to the one via circuits, it was lower by 309.8 mA for the mean and 286 mA for the median, resulting in a mean of 8.2195 A and median of 8.1535 A indicating ten via circuits having the lowest performance in maximum current resulting in reduced reliability. A difference of 0.066 mA between the mean and median indicates there are few outlying results with the maximum current of the ten via circuits. The standard deviation was also lower compared to the five via circuit by 47.2 mA but was higher compared to the one via circuit by 26.2 mA, resulting in a standard deviation of 0.3983; this indicates the maximum current measurements were closer to the mean compared to the five via circuits while being further away compared to the one via circuits.

Table 4.2: Results of the maximum current testing.

	One Via	Five Via	Ten Via
Number of samples	80	80	80
Mean maximum current	8.5293 A	8.6562 A	8.2195 A
Median maximum current	8.4395 A	8.6360 A	8.1535 A
Standard deviation	0.3721 A	0.4455 A	0.3983 A

Figure 4.1. is a box and whisker plot of the statistical data used to create Table 4.2; it shows how the maximum current measurements are distributed for each of the three circuits, with the quantities of one, five and ten vias. The one via circuit plot shows that the lower and upper quartile are close to the median with a range of 8.3195 A – 8.6755 A (0.356 A) and a minimum and maximum range between 7.903A - 9.206 A (1.303 A) with four clear outliers. The five via circuits plot shows the lower and upper quartile are further away from the median compared to the one via circuit; the lower quartile at 8.3325 A is close to the lower quartile of one via; this indicates that 75% of maximum current for both the one via and five via was above 8.32 A, with the five via upper quartile being at 9.206 A making the range for 50% 0.624 near doubling compared to the one via at 0.356 A. The minimum and maximum range for the five vias is at 7.7190 A – 9.6120A (1.893A); this indicates that while the maximum current was higher on average and with the median, the range of maximum current was greater compared to the one via circuit, the one via circuit would have a higher chance of it failing closer to the median.

The ten vias circuit box plot in Figure 4.1 shows how lower the maximum current mean and median are compared to the one and five via circuits. The ten via circuits mean and the median is lower than the lower quartile for the one and five via circuits, indicating more than 50% of the current values fall below 25% of the other two circuits. The total range between 7.4400 A – 9.4400 A is 2A, which is slightly greater than the five via at 1.893 A; this shows that the more vias on the circuit increase the range at which the maximum current can occur. The range between the lower quartile 7.924 A and the upper quartile 8.5315 A at 0.6075 A is near the

range of the five via circuits; this indicates that 50% of the values distribution range does not change going from five vias to ten vias.

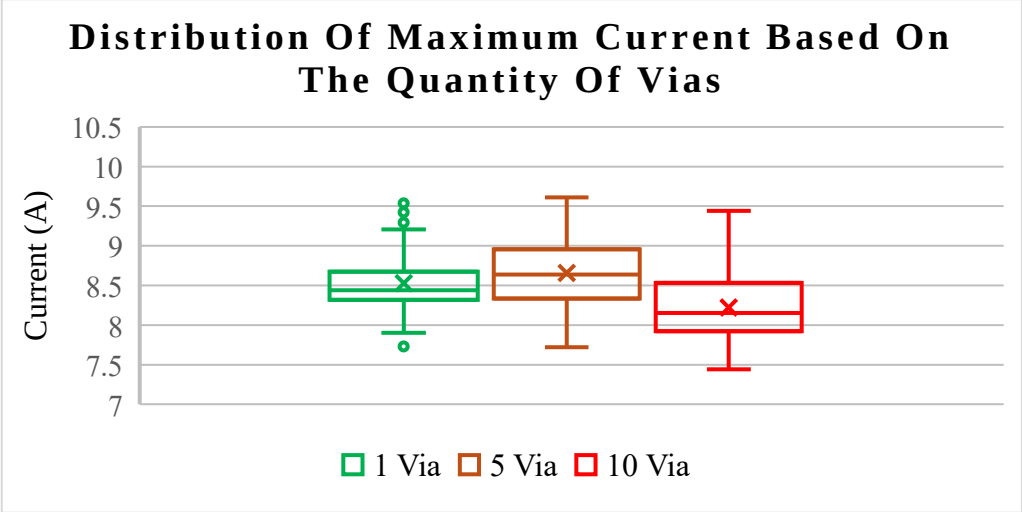

Figure 4.1: Box plot of the three types of circuits showing the distribution of the maximum current reached.

Further investigation was conducted to look at the maximum current of each type of circuit individually; Figure 4.2 shows the distribution of the maximum current for each of the different via circuits. The histogram shows a Gaussian distribution with a minor positive skewing, with the peak at 8.4 ± 0.1 A with 17 reoccurrences. The histogram shows that 8.3 A and 8.5 A made up 40 of the failed circuits, with maximum current making up 50%, indicating how central the failure would occur around the median, as previously identified.

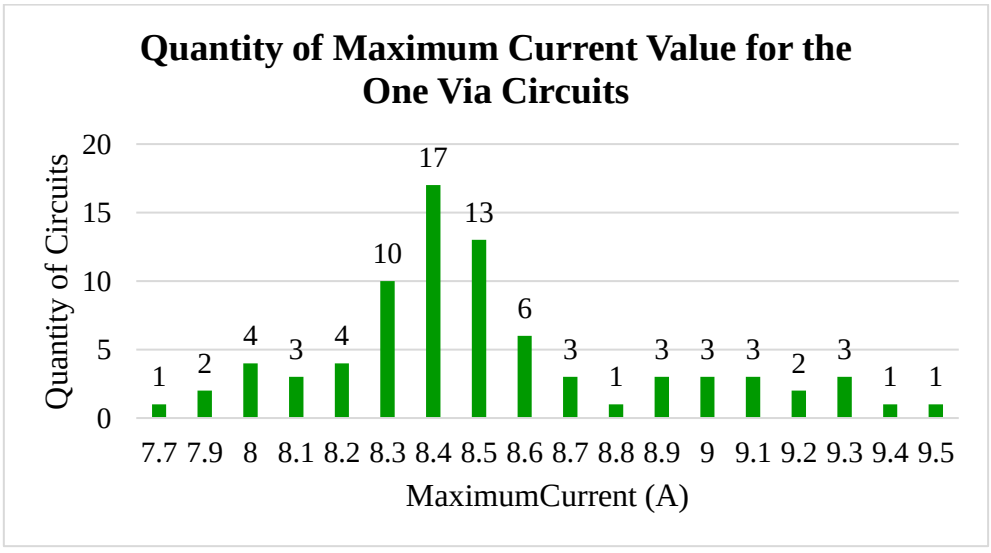

Figure 4.2: Histogram of the quantity of maximum current values for the one via circuits.

For the five via circuits, the distribution of the maximum current based on the quantity is significantly different compared to the one via circuits, as shown in Figure 4.3; the histogram shows it still has a Gaussian distribution and is not positively or negatively skewed with its centre being at 8.6 A, slightly higher than the one via circuits. The Gaussian profile is also a lot flatter as the distribution is more spread out across the various maximum current values, with 53% of the values laying between 8.3 A and 8.8 A, making the range 0.5 A, when compared to the one via circuits 50% range of 0.2 A.

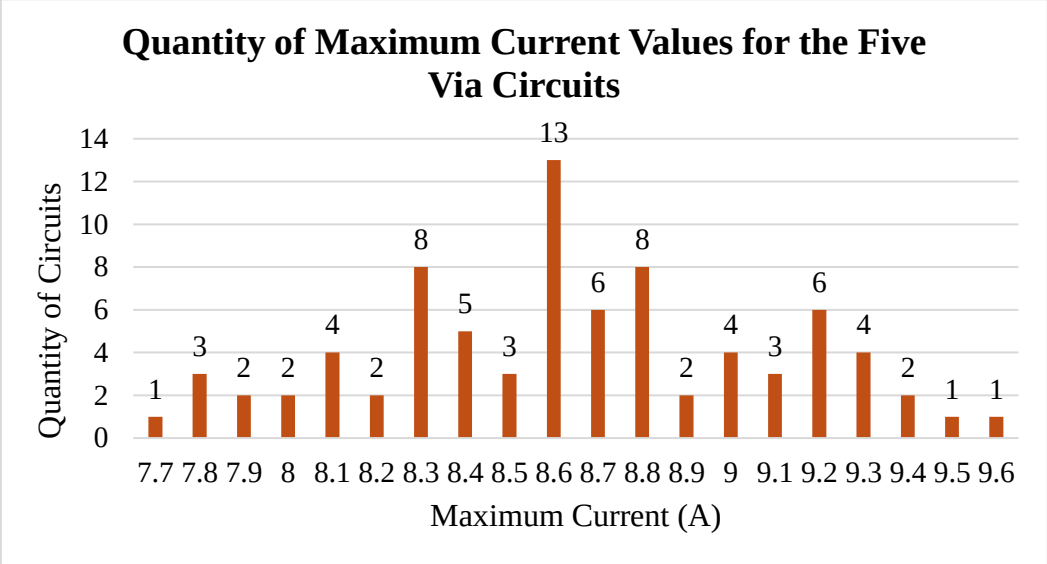

Figure 4.3: Histogram of the quantity of maximum current values for the five via circuits.

Similar to the one and five via circuits, the ten via circuits' maximum current distribution based on quantity also has a Gaussian distribution pattern, as shown in Figure 4.4. The distribution is centralised around 8.2 A with a very minor positive skew; this is because 50% of the values fall between 7.9 A and 8.2 A, and this range of 0.3 A falls between the five via circuit at 0.5 A and one via circuit at 0.2 A, as was identified previously, this indicates that the maximum current of the ten via circuits like the five via circuits is more spread out over the range of currents.

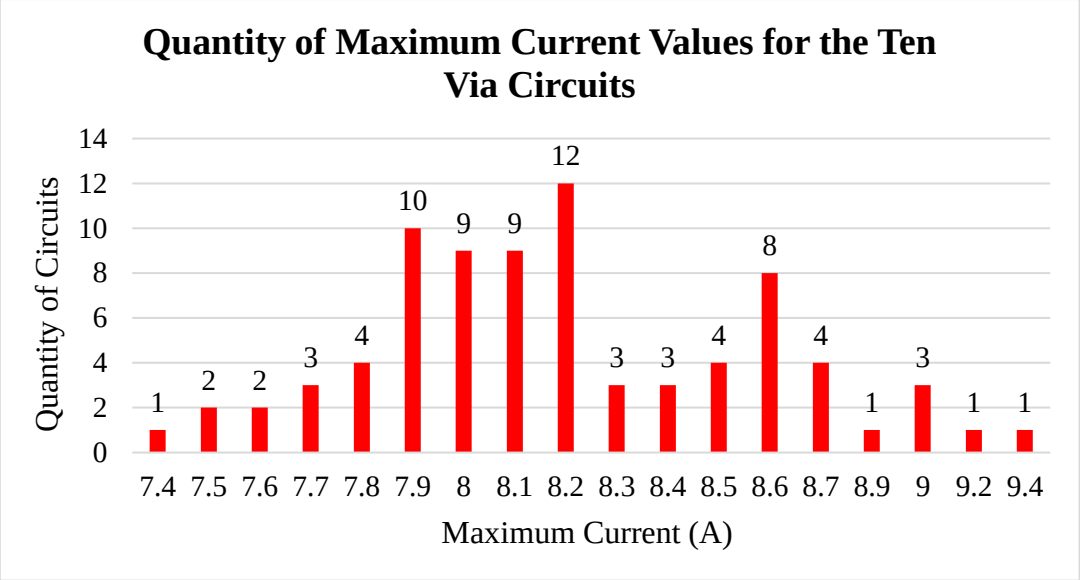

Figure 4.4: Histogram of the quantity of maximum current values for the ten via circuits

4.3.2 Maximum Current Summary

The experiment of maximum current results has shown that going from one to five via circuits, the reliability of the circuits improves based on the mean, median and maximum values; this improvement comes at the expense of a less predictable model, as the maximum current range has increased by approximately 70%. When the circuits go from five vias to ten vias, the inverse happens, and the reliability degrades based on the mean, median, maximum, and minimum values, and similar between the five vias, the predictability decreases as the spread between the maximum and minimum increases from the five via circuits. These results indicate, based on the aim of this dissertation, that when it comes to maximum current, increased quantities of vias decrease the reliability of PCB circuits.

4.4 Thermal Properties

4.4.1 Results

Following the maximum current experiment was the thermal properties experiment; Table 4.3 shows the results of the thermal properties of the one via circuits, where all circuits failed. The one via circuits shows the lowest starting value at 87.344°C for the mean and 85.000°C for the median with a standard deviation of 14.351°C, with all circuits reaching the current of 5.0 A. Table 4.3 shows that as the current increases, the temperature increases exponentially until 9A, then it levels out; the difference between the mean and median also increases alongside the

temperature increase. The standard deviation increases per 500 mA, up until it reaches 8.0 A, maxing out at 39.683°C; after this current, the circuits start to fail, and the standard deviation also begins to decrease; what this indicates is that as the current increases the temperature of the circuits have a larger range, making it less predictable. The sudden drop in the standard deviation is due to multiple circuits reaching the maximum readings of the FLIR i5 camera, levelling out values at 8.5 A, and 34 circuits reaching +270°C. Table 4.3 also shows that most of the circuits failed after 9.0 A, where more than half the remaining circuits would reach +270 °C at each current value, with only ten circuits reaching 10 A before failure.

Table 4.3: Thermal experiment results for circuits with one via.

One Via Circuit					
Current	Mean Temperature	Median temperature	Standard deviation	Samples Reached current	Samples Reached 270°C
5.0 A	87.344 °C	85.000 °C	14.351 °C	80	0
5.5 A	93.918 °C	92.000 °C	15.712 °C	80	0
6.0 A	105.462 °C	103.000 °C	18.473 °C	80	0
6.5 A	121.964 °C	117.500 °C	20.404 °C	80	0
7.0 A	144.525 °C	140.500 °C	25.375 °C	80	0
7.5 A	171.150 °C	160.500 °C	31.677 °C	80	0
8.0 A	205.588 °C	192.500 °C	39.683 °C	80	8
8.5 A	235.487 °C	237.000 °C	34.970 °C	78	34
9.0 A	256.191 °C	270.000 °C	20.527 °C	63	36
9.5 A	268.839 °C	270.000 °C	3.882 °C	31	28
10.0 A	270.000 °C	270.000 °C	0.000 °C	10	10
Total samples	80 (4 PCBs x 20 Circuits)				

With the one via circuit results established as the control values, the results produced in Table 4.4 for the five via circuits can be compared. The first area of change is the starting temperature at 5 A; for the one via circuits, it was 87.344 °C for the mean, 85.000 °C for the median with a standard deviation of 14.351 °C, while the five via is at 117.788 °C for the mean, 117.000 °C for the median with a standard deviation of 11.350 °C. The increase in temperature can be explained by the resistance of the circuit that was produced in Table 4.1, as well as Equations 1.2 and 4.1, as the additional vias add resistance to the circuits, in turn, increasing the power loss of the circuit as thermal energy; furthermore, there is also the impact of via fields identified by (Slee et al., 2009) where the closeness of the vias and current impact the neighbouring vias, increasing the temperature.

Table 4.4 also shows that no circuit reached 9.5 A, indicating that all the circuits failed before this current level; failure of the circuits started to happen between 7.5 A to 8.0 A, with four failing before 8.0 A, similar to the one via circuits once circuits reached +270°C failure would follow as indicated with 19 reaching 270 °C at 7.5 A. Only nine circuits reached 9.0, and none reached 9.5 A, with more than half failing between 8.5 A and 9.0 A. Compared to the one via circuit in Table 4.3, which had 63 circuits reach the maximum current that the five via circuits achieved. This higher temperature is one explanation for why the five via circuits fail at lower current values; another is the circuit design, with the alternating pattern of the circuit due to the odd number of vias, which results in a trace between the vias and pads on both sides of the PCB, and with these traces being the weakest location on the circuit (see Section 4.4.1), reducing the area the vias can dissipate heat too without impacting the traces.

These results for the five via circuit, when compared to the one via circuits, do not match the results (Coppola et al., 2008) found, where the one via circuits had a lower maximum current at higher temperatures, while the five via circuits had a higher maximum current at lower temperatures indicating that DC does not have the same impact as a single phase of AC. Alternatively, it could indicate the difference between the layout of the vias, that the impact of vias in series as used in this dissertation does not match those that are in parallel as were used in (Coppola et al., 2008) . These results indicate that the five via circuits had reduced reliability compared to the one via circuits, indicating that the increase in vias is detrimental to the reliability.

Table 4.4: Thermal experiment results for circuits with five vias.

Five Via Circuit					
Current	Mean Temperature	Median temperature	Standard deviation	Samples Reached current	Samples Reached +270°C
5.0 A	117.788 °C	117.000 °C	11.350 °C	80	0
5.5 A	125.948 °C	124.000 °C	11.807 °C	80	0
6.0 A	144.038 °C	142.500 °C	14.684 °C	80	0
6.5 A	169.763 °C	168.500 °C	17.495 °C	80	0
7.0 A	205.663 °C	202.500 °C	22.140 °C	80	0
7.5 A	245.475 °C	243.000 °C	21.053 °C	80	19
8.0 A	268.539 °C	270.000 °C	5.082 °C	76	67
8.5 A	270.000 °C	270.000 °C	0.000 °C	57	57
9.0 A	270.000 °C	270.000 °C	0.000 °C	9	9
9.5 A	N/A	N/A	N/A	0	0
10.0 A	N/A	N/A	N/A	0	0
Total samples	80 (4 PCBs x 20 Circuits)				

Table 4.5 shows the temperature at each current level for the ten via circuits; when these values are compared to the five via circuits in Table 4.4, the temperature difference at the start is negligible, being on average at 5 A, 120.221 °C for the ten vias higher when compared to 117.778 °C for the five vias making a difference of 3 °C, similar when it comes to the median temperatures, with ten via at 113.5 °C and five via at 117.0 °C with a 3.5 °C difference. As the current increases, the difference in temperature increases as well; at 7.5 A, the ten via circuits temperature on average was 214.163 °C which is lower when compared to the five via circuits at 245.475 °C which is a 31.312 °C difference, compared to the 3°C difference at 5 A, A similar pattern with the median temperature at 7.5 A with ten vias circuits with 217.5 °C and five vias at 243.0°C with a 25.5 °C difference.

The standard deviation of the ten vias circuits shows that the temperature between each circuit is inconsistent. Table 4.5 shows that the standard deviation is consistent between 24-30 °C for the majority of current levels, compared to five vias in Table 4.4, which is more consistent with its temperature with a standard deviation between 11-22 °C; this reduction in consistency makes the ten via circuit less predictable based on the temperature at different current values. Furthermore, as found by (Beng et al., 2013), an increase in the quantity of via reduces the surrounding FR-4 dielectric thermal resistivity, allowing more heat energy to be transferred to the surface area of the FR-4 dielectric. Leading to the final observation between the ten via and five via circuits, that the ten via circuits, while having near the same temperature, have more circuits reach the maximum current of 10 A of the experiment, with the first failure happening between 8.0-8.5 A, while the five via have the first failures between 7.5-8.0 A. This capability of the ten vias to hold higher temperatures longer can be attributed to the fact that on one side of the PCB, the only traces are between the via; this allows the heat to dissipate to the surface area of the bottom layer without impacting the trace between the vias and pads in effect making the vias act similar to thermal vias (Bogatin, 2021).

When the ten via circuits temperatures in Table 4.5 is compared to the temperature of the one via circuits in Table 4.3, it is clear that the one via has the lowest temperatures, going from 5A to 10 A, for both the average and median temperatures, indicating that having the lowest quantity of vias is optimal to minimise the amount of heat produced by the circuit. However, the increase in vias allowed more heat to be transferred to the dielectric by reducing the resistivity, as found by (Beng et al., 2013), allowing more circuits to survive to the maximum current.

Table 4.5: Thermal experimental results or circuits with ten vias.

Ten Via Circuit					
Current	Mean Temperature	Median temperature	Standard deviation	Samples Reached current	Samples Reached 270°C
5.0 A	120.221 °C	113.500 °C	24.126 °C	80	0
5.5 A	128.513 °C	121.000 °C	26.929 °C	80	0
6.0 A	143.900 °C	137.500 °C	30.526 °C	80	0
6.5 A	163.200 °C	158.500 °C	29.025°C	80	0
7.0 A	188.000 °C	187.000 °C	27.899 °C	80	1
7.5 A	218.163 °C	217.500 °C	28.105 °C	80	6
8.0 A	248.425 °C	256.000 °C	24.149 °C	80	32
8.5 A	267.215 °C	270.000 °C	7.067 °C	79	63
9.0 A	270.00 °C	270.000 °C	0.000 °C	67	67
9.5 A	270.00 °C	270.000	0.000 °C	50	50
10.0 A	270.00 °C	270.000	0.000 °C	33	33
Total samples	80 (4 PCBs x 20 Circuits)				

Figure 4.5 below shows how the temperature process over the current range for each of the PCB cards tested in the experimentation for each of the three circuit types one, five and ten vias, which displays a pattern like a Sigmoid function (Chakraverty, 2020), it starts flat, then the temperature rapidly rises as the current increases, then plateaus at +270 °C to the limitation of the Flir i5 thermal infrared camera. Figure 4.5 illustrates how the one via circuits has the lowest temperature profile for each of its PCBs, with only one card having all its circuits fail before 10 A. Furthermore, Figure 4.5 also shows how similar the temperatures between the five via PCBs and ten via PCBs are, with both circuit types showing the same temperature pattern overlapping, and when it reaches between the 7-7.5 A range, then the five via circuits start to have an increased temperature profile as also shown between Table 4.4 and 4.5. The five via circuits plot shows at least two cards (cards 3 and 4) failing, as all cards failed before the 10 A maximum; the other two cards (cards 1 and 2) are overlapped by the two shown. The only circuit type to fail before 10 A in Figure 4.5 is the one via circuit, specifically card 1, which is unclear in Table 4.5. Another factor that is shown is that the ten via circuit temperature over the current range is a lot more sporadic between the cards when compared to the one and five via circuits, which are more consistent between each card; this shows that the ten via circuits are less predictable in their temperature compared to the other two circuit types.

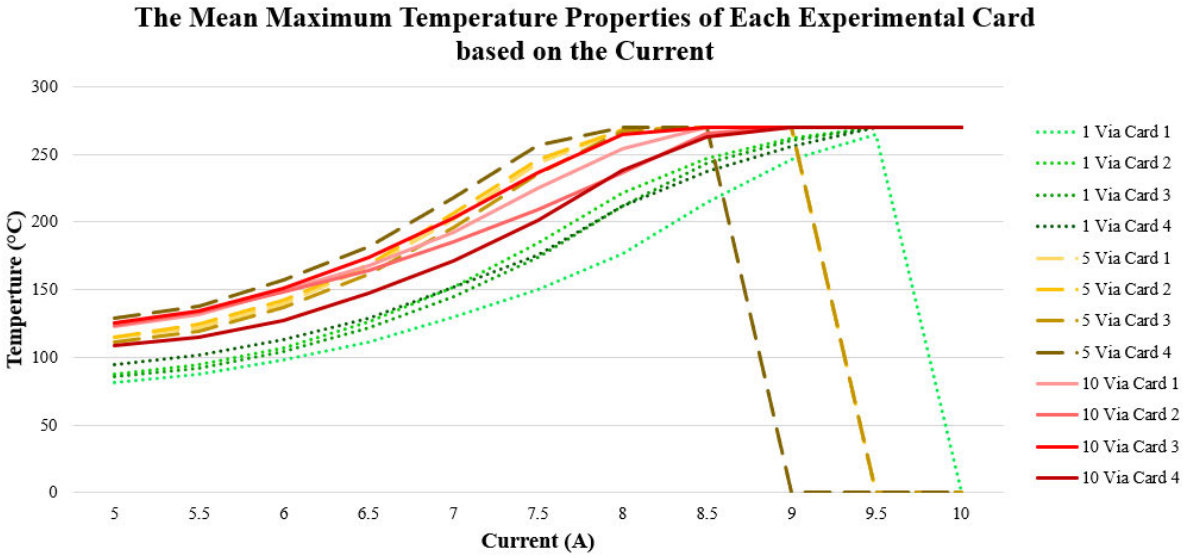

Figure 4.5: The plot of the mean temperature properties of each experimental card over the range of currents with green dots being one via, yellow dash dot being five vias and red solid line for ten vias.

While the temperature was recorded for statistical analysis, thermal images of the circuits were also taken at each current level to show the thermal pattern for each type of circuit visually. Figure 4.6 shows the one via circuit thermal profile; the thermal profile is focused on the trace as the shape is tear-shaped with the bulb toward the left alligator clip, and this pattern persists throughout all the images. The shape indicates that the heat is concentrated on the trace between the pad and via, not on the single via of the circuit. The overall area of the thermal profile is shown to be consistent up until (j), where it starts to expand (k) just before failure occurs (l); the expansion indicates the surrounding area has reached its limit in the heat it can dissipate and require more area to dissipate more heat from the circuit. Due to the limitation of the thermal camera capturing images of only one layer, the bottom layer's thermal profile cannot be seen, limiting the overall thermal profile of the one via circuits.

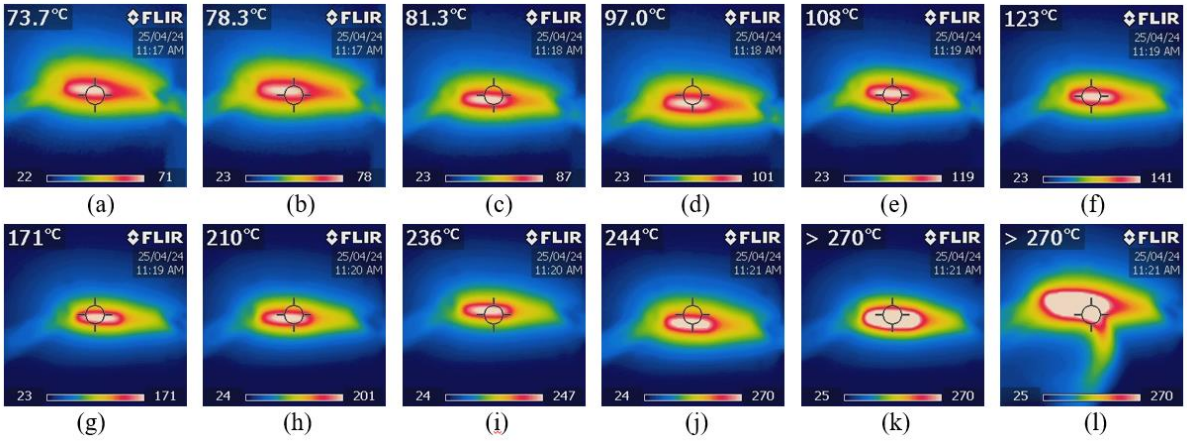

Figure 4.6: Thermal images of a circuit with one via at (a) 5.0 A, (b) 5.5 A,(c) 6.0 A, (d) 6.5 A, (e) 7.0 A, (f) 7.5 A, (g) 8.0 A, (h) 8.5 A, (i) 9.0 A, (j) 9.5 A, (k) 10 A and (l) after failure.

The five via circuits show a different thermal profile compared to the one via circuits in Figure 4.7; the highest temperature is more centred on the circuit between the alligator clips; this shows that the vias are the central point for the temperature to focus around, with the central vias emitting the highest temperatures. Similar to the one via, the thermal profile maintains the same shape up until it gets closer to failure; in Figure 4.7 (h), the thermal profile starts to shift more toward the left alligator; this is more profound in (i), which would indicate that the trace temperature matches the vias temperature. The areas of the five via circuits' thermal profile are increasing at this stage, similar to the one via circuit. The point just after failure in Figure 4.7 (j) is slightly larger in the area it occupies compared to Figure 4.6 (l), but this could be explained by it being captured while the FR-4 dialect is still burning off.

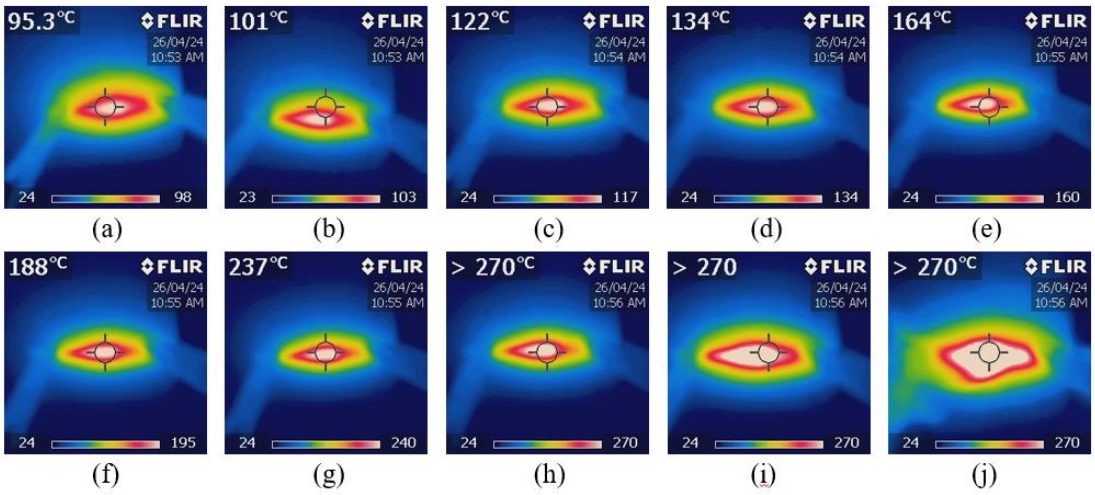

Figure 4.7: Thermal images of a circuit with five via at (a) 5.0 A, (b) 5.5 A, (c) 6.0 A, (d) 6.5 A, (e) 7.0 A, (f) 7.5 A, (g) 8.0 A, (h) 8.5 A, (i) 9.0 A and (j) after failure.

Figure 4.8 below is the thermal profile of the ten via a circuit, which has a more oval shape compared to the one and even five via circuits in Figure 4.6 and 4.7; the profile demonstrates the concentration of the temperature is around the ten vias, with the temperature hottest towards the central vias; the oval shape also has a thinner profile along the circuits compared to the previous circuits, indicating the temperature has a larger area for the heat to dissipate into the surround FR-4 dielectric, this increase in the area can be attributed to the reduced thermal resistivity caused by the quantity of vias (Beng et al., 2013). Similar to the other circuits, the ten via circuits maintain the thermal profile up until (i) in Figure 4.8, where the profile starts to expand, indicating the heat needs more area to dissipate into; it continues to expand through (j) and (k) until failure in (l), here the profile has slightly more area than (j) in Figure 4.7 for the five via circuit, this can just be seen comparing the alligator clips on the right in both Figure 4.7 and 4.8, which shows a greater width against the circuit.

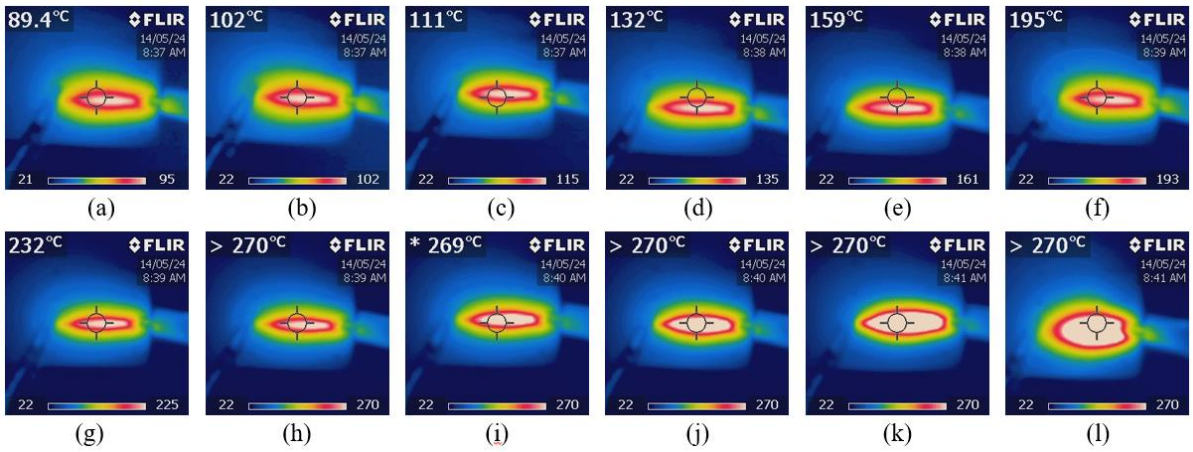

Figure 4.8: Thermal images of a circuit with one via at (a) 5.0 A, (b) 5.5 A, (c) 6.0 A, (d) 6.5 A, (e) 7.0 A, (f) 7.5 A, (g) 8.0 A, (h) 8.5 A, (i) 9.0 A, (j) 9.5 A, (k) 10 A and (l) after failure.

4.4.2 Thermal Properties Summary

The results from the thermal experimentation demonstrate the thermal properties of circuits containing either one, five or ten vias as the current increases from 5 A up until either 10 A or failure occurs. The statistics show that the overall temperature of the circuits increases the quantity of vias from one to five but remains close between five and ten vias. Even with the five and ten via temperatures remaining close, the five vias had reduced reliability, failing earlier than the ten vias, which could hold higher temperatures longer than the five vias. While the ten vias could hold the temperature longer, showing in one is improved reliability, this heat could impact other circuits, components, or internal layers on PCBs that the circuit shares, which is more common in today's PCB designs, indicating when it comes to temperature, the reliability would be just as negative as the five via circuits.

Furthermore, concerning reliability, the thermal images show that the one via circuit had a better thermal profile, occupying less area compared to the five and ten via circuits, with its performance in its temperature being overall lower than the five and ten vias, the one via circuits performed the best when it comes to thermal consideration with the reliability of the PCB.

4.5 Comparison Between the Maximum Current and Thermal Experiment Results

While the maximum current and thermal experiments were separate, there is overlap between the two, as both are based on current levels and the overall impact of heat energy through losses by Joule's law (Equation 2.1).

When comparing the one via circuits, maximum current results in Figure 4.2, to the thermal results in Table 4.3 it is observed that more circuits reach higher values of current in the thermal experiment; in Figure 4.2, only 1 circuit reaches 9.5 A, and zero reaches 10 A, while in Table 4.3, 31 reached 9.5 and 10 reached 10 A. This comparison is also observed with the ten via circuit when comparing the results in Figure 4.4 with the results in Table 4.5, where not one circuit reached 9.5 A in the maximum current experiment, while 50 reached 9.5 A and 33 reached 10 A for the thermal experiment. Both observations indicate that the methodology between the experiments is to explain this discrepancy, with the major factor being the time to rest between current increments. As the current increases, more heat energy is generated as per Joule's law (Equation 2.1); for this heat to dissipate into the surrounding mediums, it requires time for the temperature to balance out, the thermal experiment with its 20 seconds of rest between increments allow more time for the heat to be transferred to the surrounding medians, specifically the FR-4 dielectric. The smaller current (100 mA) and time increments (5 seconds) in the maximum current experiment do not allow the consistently increasing heat energy time to disperse and level out the temperature, containing the heat within the copper elements of the circuit, leading to failure earlier.

The exception is with the five via circuits; comparing the results in Figure 4.3 with the results in Table 4.4, there are only minor discrepancies between failures at the current levels, with 50 circuits reaching above 8.5 A in Figure 4.3 compared to 57 reached 8.5 A in Table 4.4. This demonstrates that the methodology did not impact the five via circuits in a similar means as the one or ten via circuits. With the greater temperature caused by the five vias compared to the one via circuit and the circuit and having the trace between via and pads on both sides reducing the area to dissipate the heat when compared to the ten via circuits, this causes the trace between the pad and vias on either side to reach breaking point in q quick time frame causing the failure to occur at similar currents in both experiments.

4.6 Physical Properties of Failure

To observe if the quantity of vias had an impact on the reliability of PCB, the physical properties of the failure were observed; this was broken down into three areas:

- Failure location
- The physical changes towards failure
- Area of destruction after failure

4.6.1 Failure Location Results

Through both the maximum current and thermal experiments, failure occurred 99.375% of the time on the traces, specifically the traces between the via and pads, as shown in Figure 4.9 with 160 failures on the trace for one via circuit, 159 for five via circuit and 158 for ten via circuits. The two via failures occurred when the via plating fell out of the circuit, indicating that the connection between the plate and dielectric had failed due to the heat.

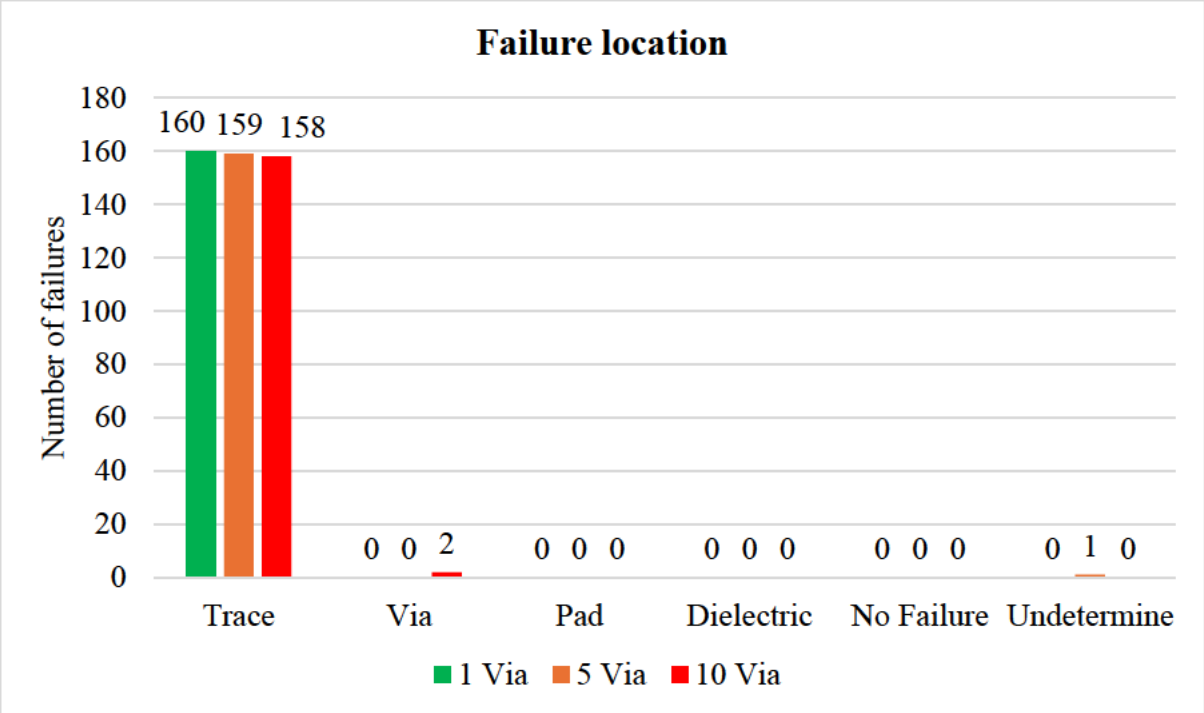

Figure 4.9: Histogram of the quantity of failure locations.

The reason why the trace is the primary failure location is due to the cross-sectional area difference between the trace and via; the cross-sectional area is calculated using Equation 4.2, and the values from Table 3.1 for the trace where W is the trace width, and L is the trace thickness resulting in a cross-sectional area of 0.0107 $mm^{2,}$ while the via is calculated using Equation 4.3 with the inner diameter of the via being r_1 and the hole plating thickness being r_2 resulting in the cross-sectional area of 0.0159 mm^2.

$$A_{rectangle} = L*W \tag{4.2}$$

Where: $A_{rectangle}$ is the cross-sectional area of a rectangle (m^2);
L is the length of the rectangle (m);
W is the width of the rectangle (m)

$$A_{tube} = \pi(r_1^2-r_2^2) \tag{4.3}$$

Where: A_{tube} is the cross-sectional area of the tube[via] (m^2);
r_1 is the outside radius of the tube (m);
r_2 is the inside radius of the tube (m)

This difference of 0.0052 mm^2 for the cross-sectional area allows the via to transfer more heat to the surrounding area, consequently reducing the temperature of the vias based on heat transfer of conduction as per Equation 1.1.

4.6.2 Physical Changes Towards Failure Results

Physical images were taken to capture the physical changes as the circuits lead up to failure during the thermal experiment at each current level; due to limitations of the number of cameras being used, the images are only of the top layer, with only speculation that the bottom layer experience similar physical changes. Figure 4.10 shows the PCB board with one via circuits as the current is increased from (a) 5 A to (k) failure; for the first several images (a) to (g), there is no identifiable change in the physical properties of the PCB or circuit, in the image (h) a white outline appears around the circuit as the heat from the circuit is starting to impact the surrounding FR-4 dielectric. As the current is increased to 9 A in (i) of Figure 4.10, the trace of the circuit darkens in colour as it starts to burn; as the current is increased to 9.5 A (j), the

surrounding FR-4 dielectric is now darkened which indicates it is burning, melting and it is FR-4 dielectric structure is starting to degrade in a rapid rate similar to (Polanský et al., 2014) findings due to the increased heat; additionally the trace between the via and pad glows a hot red colour. The trace glows a white-hot when the current reaches 10 A shown in (k) of Figure 4.10, and the dielectric area being impacted by the heat is increased; once the trace is hot white, this was an indication the circuit was about to fail. When failure occurred with the circuit, the trace would fail first, triggering the dielectric to ignite and catch on fire, as shown in Figure 4.10 (l) showing the point of failure.

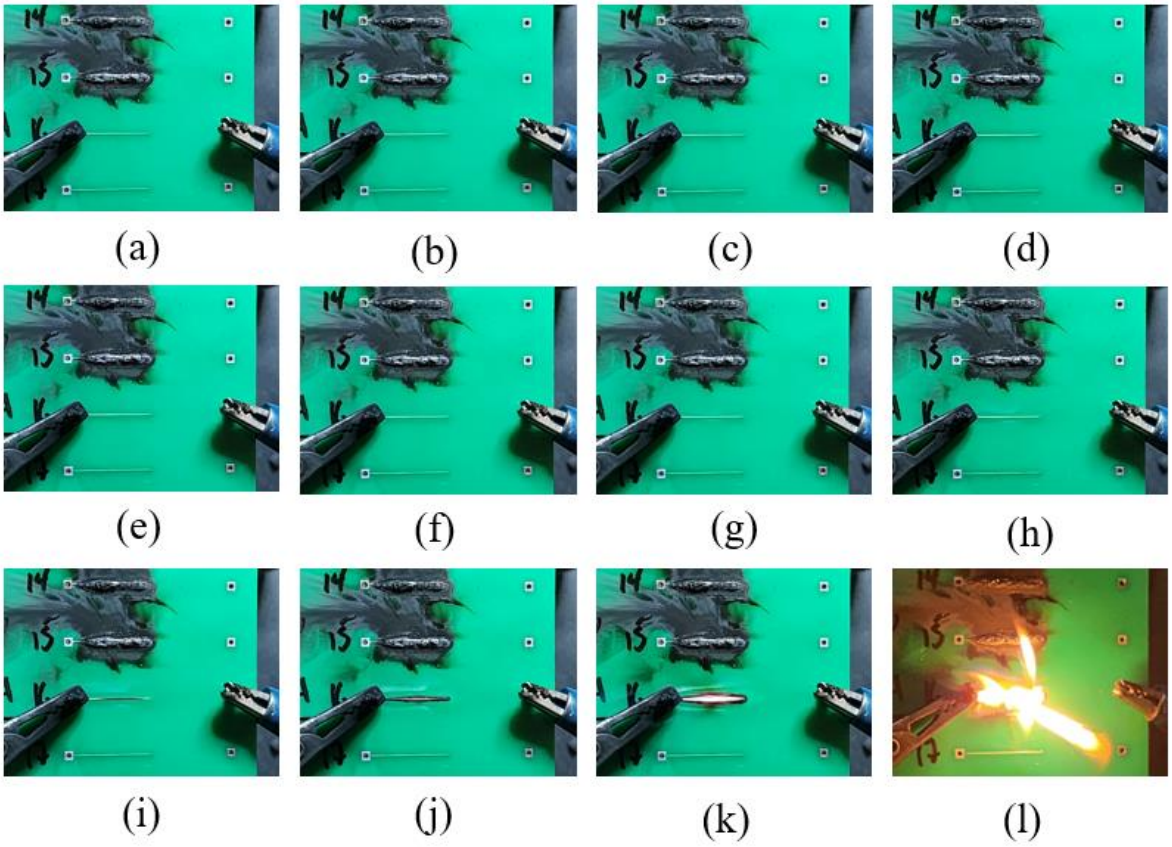

Figure 4.10: Photos showing the physical impacts caused by the temperature at (a) 5 A, (b) 5.5 A, (c) 6 A, (d) 6.5 A, (e) 7 A, (f) 7.5 A, (g) 8 A, (h) 8.5 A, (i) 9 A, (j) 9.5 A, (k) 10 A, (l) failure for one via circuit, PCB card 2, circuit 16.

The Five via circuit initially performs similarly to the one via circuit in regards to the physical impacts; in Figure 4.11, through b(a) to (c), there is no noticeable change in the physical properties, then through (d) to (g) the colouration of the surrounding FR-4 Dielectric changes from a darkened shadow to a white that is focused around the vias, compare to the trace with the one via circuits. The next stage of the changes in Figure 4.11 happens at (h) 8.5 A, where

the dielectric surrounding the vias darkens in colouration as well as the trace leading towards the pad on the left, the dielectric impacted by the temperature has increased in the area indicated by the white area, the final stages as shown in (i) at 9.0 A the dielectric has risen due to swelling around the via and trace, and the traces in between the vias, as well as between the via and pad are glowing a red hot this is due to the greater degrading of the FR-4 dielectric structure due to the increased temperature compared to the one via circuits, the increase in degrading was identified by (Polanský et al., 2014). Figure 4.11 shows the circuit failing on the bottom layer of the PCB from the glow; this circuit had its failure occur on the traces; when the circuits fail on the bottom or top, the vias act as a gateway for the flames to transfer to the other side of the PCB causing increase area of destruction to the circuit and surrounding FR-4 Dielectric.

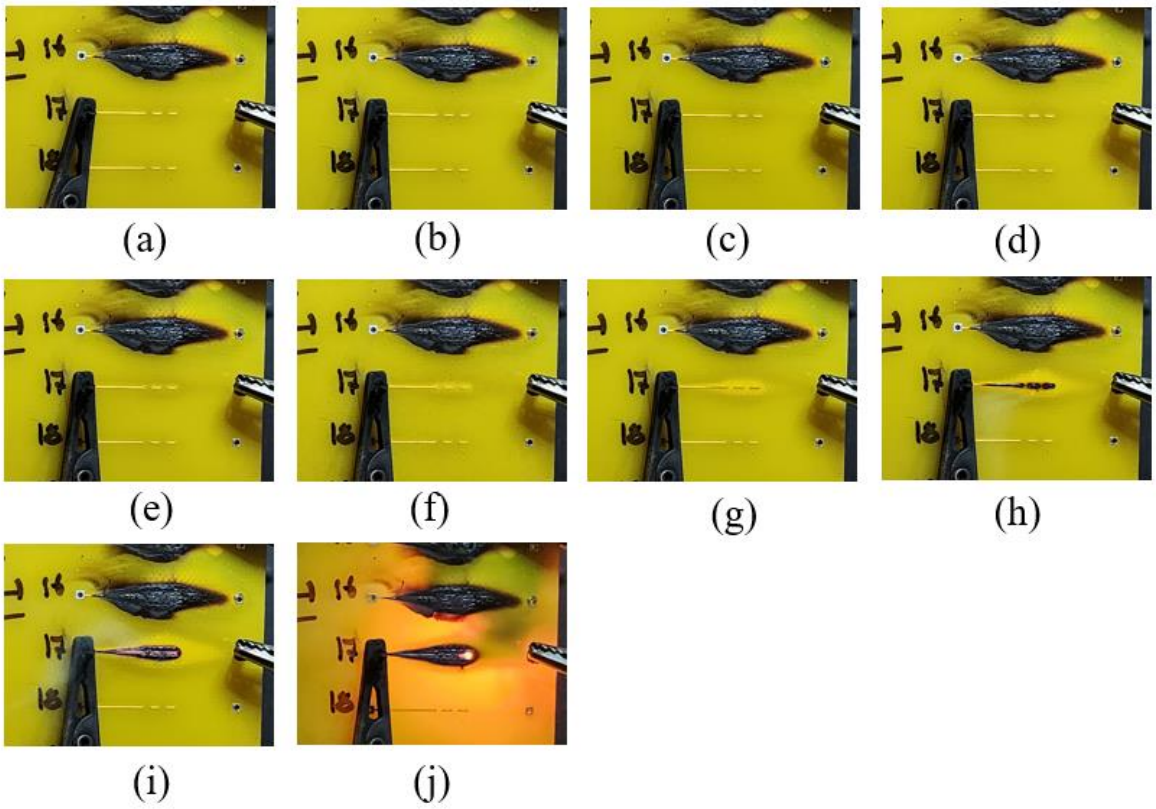

Figure 4.11: Photos showing the physical impacts caused by the temperature at (a) 5 A, (b) 5.5 A, (c) 6 A, (d) 6.5 A, (e) 7 A, (f) 7.5 A, (g) 8 A, (h) 8.5 A, (i) 9 A, (j) failure for five via circuit, PCB card 1, circuit 17.

As with the previous circuits, the ten via circuits start with no noticeable physical change in its properties between (a) 5.0 A and (d) 6.5 A in Figure 4.12, then at (e) 7.0 A, the dielectric surrounding the vias begins to darken, this darkening of the surrounding dielectric continues up until (h) 8.5 A, where the FR-4 dielectric begins to bubble near the alligator clip on the right-

hand side indicating the FR-4 has hit its boiling point. The bubbling of the dielectric rapidly spreads to vias as shown in (i) of Figure 4.12; the bubbling is unique to the ten via circuits as the one and five via circuits had no bubbling of the FR-4 dielectric; this is due to the overall increased heat dissipated into the FR-4 dielectric from the increasing number of vias as well as the breakdown of the FR-4 dielectric structure as identified by(Polanský et al., 2014); another additional change is the fumes being produced as well as it is heavily more visible in the ten via circuits compare to the other two circuits. The bubbling of the FR-4 dielectric continues to expand around the vias as shown in Figure 4.12 (j) 9.5 A, where the trace is now cloudy white hot and turns to a glowing white hot in (k), indicating the circuit is about to fail, with (l) showing the after effect of the circuit failing with the dielectric glowing red hot and expanded upwards after it has been ignited into a flame showing the damage area a single circuit can cause.

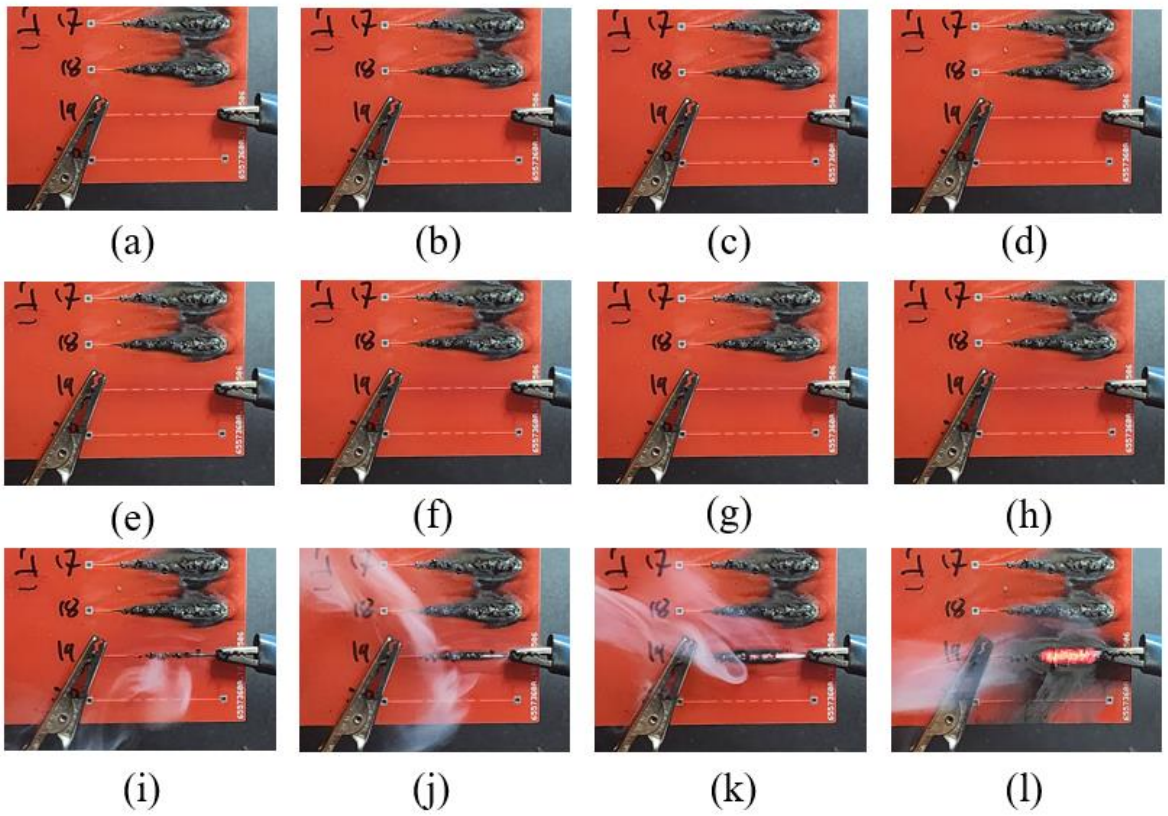

Figure 4.12: Photos showing the physical impacts caused by the temperature at (a) 5 A, (b) 5.5 A, (c) 6 A, (d) 6.5 A, (e) 7 A, (f) 7.5 A, (g) 8 A, (h) 8.5 A, (i) 9 A, (j) 9.5 A, (k) 10 A, (l) failure for ten via circuits, PCB card 2, circuit 19.

4.6.3 Physical Properties after Failure Results

One aspect of PCB reliability is the ability to do simple repairs to keep the PCB operationally functional after a failure, as this can save both e-waste and cost. When a PCB circuit or component fails, it can damage the surrounding area, including the FR-4 Dielectric, other circuits, or components on the PCB. Below in Figure 4.13 is a photo looking at two PCBs that both contain circuits that consisted of one via, one from the maximum current experiments, card 2 (a) top layer (c) bottom layer and the other from the thermal experimentations, card 3 (b) top layer and (d) bottom layer. Figure 4.13 shows that the top had significant damage to each of the circuits, especially around the trace between the via and the pad, with the dielectric breaking down into three pattern types: rectangular, teardrop and ellipse. However, the overall area is contained near the circuit, and any other circuit or component would have to be close to have a detrimental impact due to these circuits failing. The bottom layer in Figure 4.13 had a heavily reduced area compared to the top, with the majority of the circuit damage area being of a tear-drop shape, with limited damage to the actual FR-4 dielectric; the majority of the dielectric damage came from the top layer heat causing the bubbling effect seen in the white circle in Figure 4.13, for the failure to impact any other circuit or component on a similar PCB they would have to be directly on top of any these circuits. Figure 4.13 also shows that when the circuits fail, the damage is concentrated on the same layer, in this case, the top layer in the photos; in the experiment, the positive lead was always on the side that suffered the major damage.

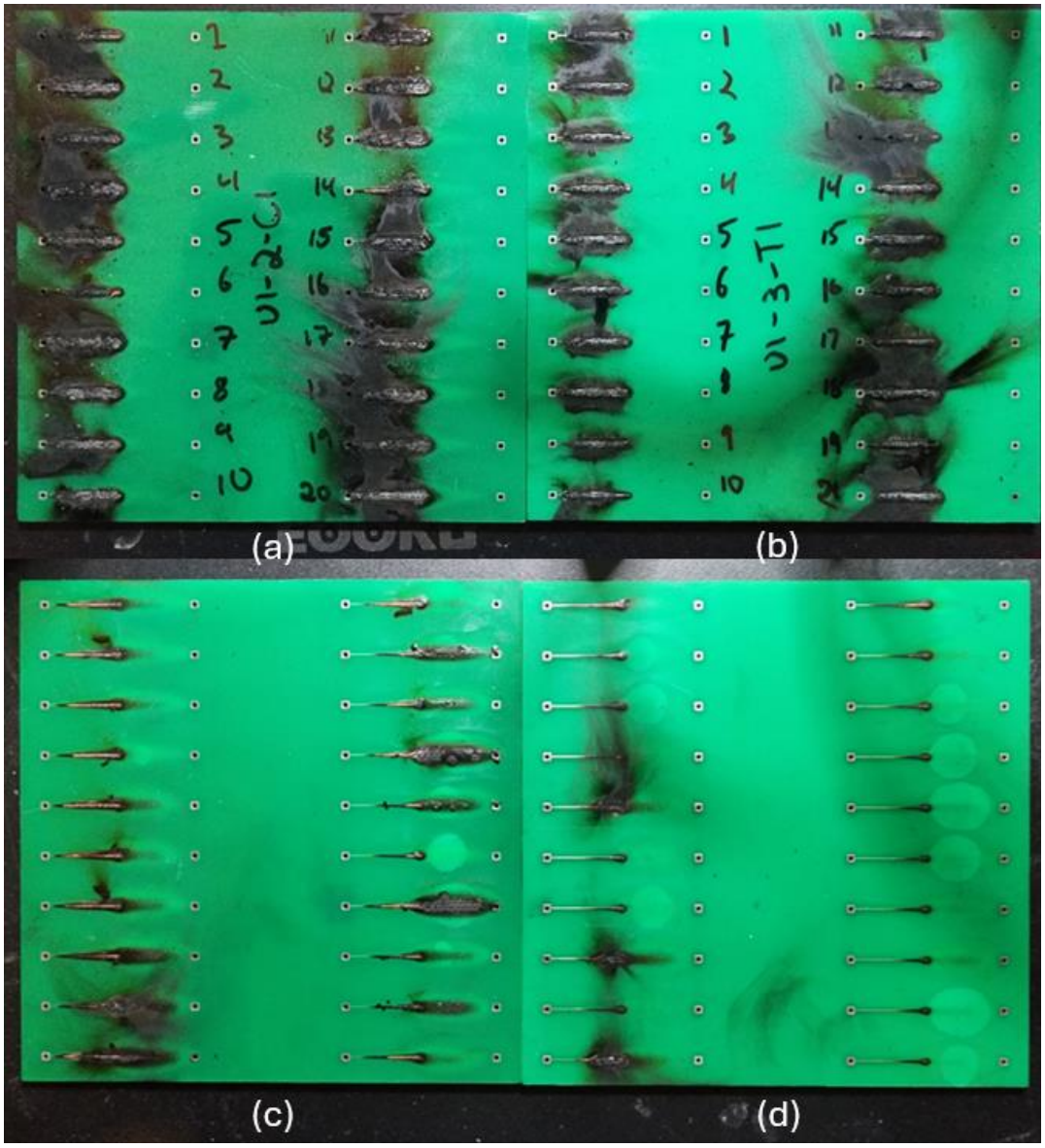

Figure 4.13: Photos of the damage caused by the failing circuits for one via from the maximum current experimentation on card 2 (a) top layer, (c) bottom layer and the thermal experimentation card 3 (b) top layer and (d) bottom layer.

The five via circuits damage in Figure 4.14 is significantly different compared to the one in Figure 4.13. it can be observed in Figure 4.14 that the top (a),(b) and bottom (c),(d) layers have both significantly more area damage caused by failure to the PCBs for both the maximum and thermal experiments, furthermore the area of damage on the top and bottom layers are approximately the same based on visuals, this indicates that failure occurred equally on both layers. As the area around each circuit is greater in Figure 4.14 compared to Figure 4.13, this indicates that there is a greater risk potential of damaging nearby circuits, components or both and limited room to re-routing the interconnection for temporary repairs.

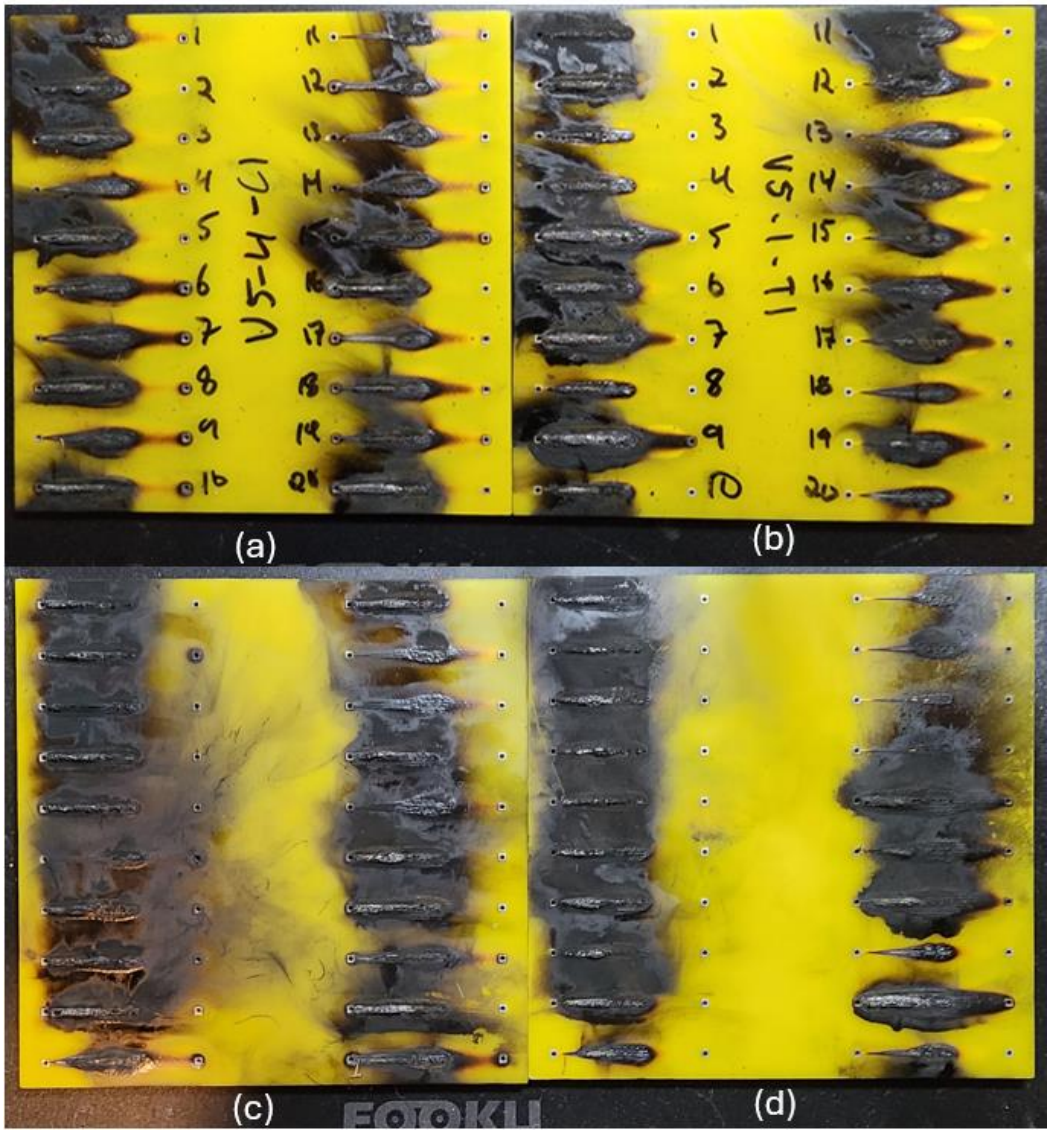

Figure 4.14: Photos of the damage caused by the failing circuits for five vias from the maximum current experimentation on card 4 (a) top layer, (c) bottom layer and the thermal experimentation card 1 (b) top layer and (d) bottom layer.

Figure 4.15 shows the damage done to two PCBs that had circuits that contained ten vias, one from the maximum current experiment card 4 (a) top, (c) bottom and from the thermal experiment card 3 (b) top layer and (d) bottom layer. When the ten via circuits in Figure 4.15 are compared to the one via in Figure 4.13 along with the five via circuits in Figure 4.14, it is clear that the ten via circuits area of damage is the largest, showing that as the quantity of via increase, the more damage will occur when failure occurs. The ten via circuits also perform similarly to the one via circuit in that most of the damage is on the top layer; for ten via circuits, this is because most of the circuit is on the top layer. Another factor is that the majority of the

damage is focused on one side of the circuits in Figure 4.15 for the top layer; the majority of the failure occurs towards the pad that has the least FR-4 dielectric area around it; this can be explained by heat conduction which is impacted by the area of the materials involved, as these sides have less area the FR-4 dielectric will reach its ignition point first before the FR-4 dielectric on the other side of the circuit.

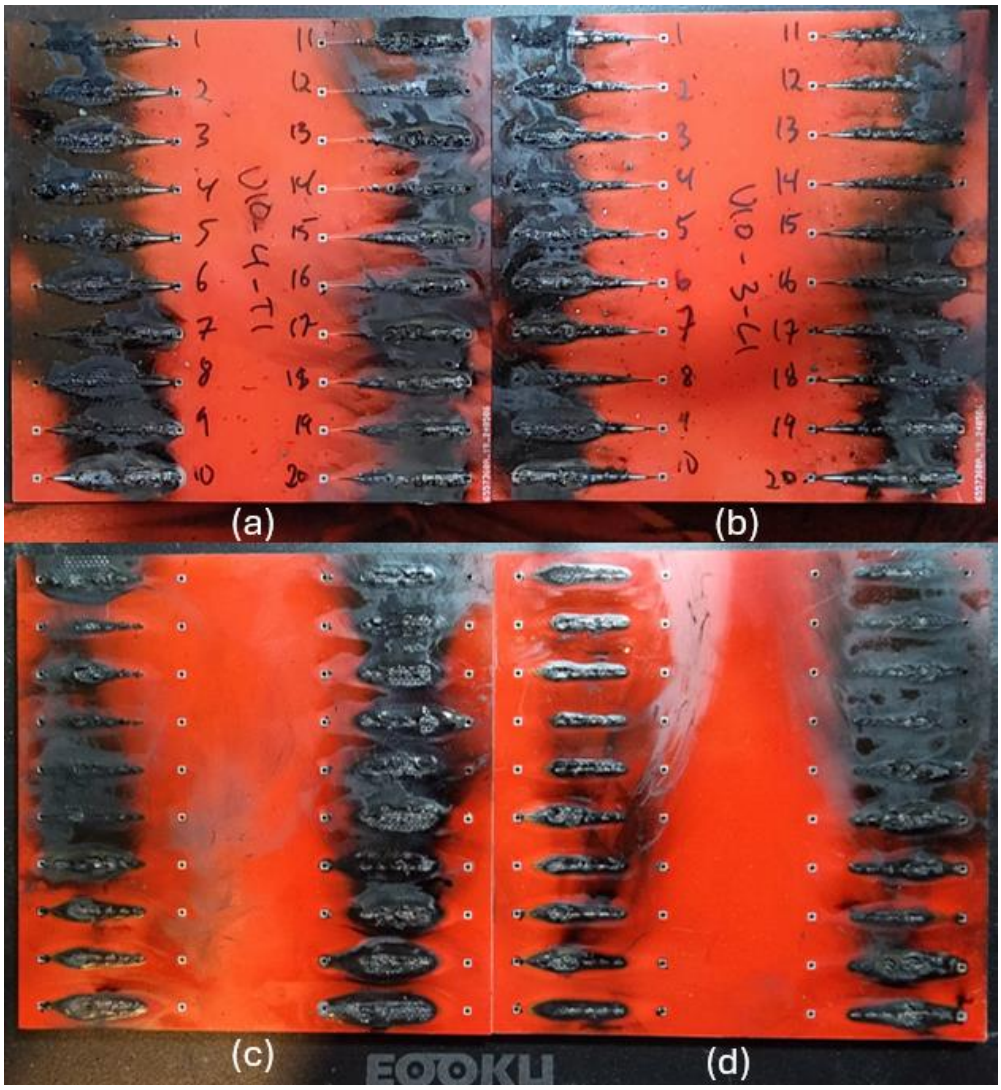

Figure 4.15: Photos of the damage caused by the failing circuits for ten vias from the maximum current experimentation on card 4 (a) top layer, (c) bottom layer and the thermal experimentation card 3 (b) top layer and (d) bottom layer.

To further confirm the increase of area, an estimation of the area of construction was carried out; there were three types of best-fit shapes to determine the equation for area: one for rectangle, one for ellipse, and the final one a tear-drop shape using a combination of a semi-circle with a triangle, the results of these calculations were produced in Table 4.6. Table 4.6 shows the area damage of the top layer, bottom layer, and total area broken down into the average, median and standard deviation of each type of circuit one, five, and ten vias in both experiments by just looking at the mean of the total area between the three circuits it is clear there is a significant difference between areas destroyed, with one via at 55.9 mm^2, five vias at 114.2 mm^2 and ten vias at 190.5 m; this shows the area doubled between each circuit type. The median of each circuit type also matches the mean with one via at 41.9 mm^2, five via at 111.1 mm^2 and ten vias at 171.1 mm^2, with each median slightly below the mean, indicating some outliers in the upper area values of the data.

As mentioned above, the one via the bottom area had, on average, less damage on its bottom layer at 21.9 mm^2 compared to 34.0 mm^2 for the top layer and similar to the ten via circuits, with the top layer having 105.5 mm^2 and the bottom layer has 85.0 mm^2 reinforcing that failure occurred on the top layer. Also, as mentioned above, for the five via circuits, the top layer and bottom layer had very similar average areas of damage between the top layer at 59.0 mm^2 and the bottom layer at 55.2 mm^2, reinforcing that failure occurred in both layers regularly. Because of the using best-fit shapes relying of eyesight and a ruler, the standard deviation for all three circuit types are significant, but do not impact the overall findings as the difference between the each circuits mean and median is significant enough to draw a conclusion from.

Table 4.6: Calculated area of damage caused by the circuits failing.

Damage Area Cause by Circuits Failing				
	Mean	Median	Standard Deviation	Number of circuits
One Via Circuit Top Area	34.0 mm^2	29.0 mm^2	23.1 mm^2	160
One Via Circuit Bottom Area	21.9 mm^2	15.8 mm^2	18.8 mm^2	160
One Via Circuit Total Area	55.9 mm^2	41.9 mm^2	34.7 mm^2	160
Five Via Circuit Top Area	59.0 mm^2	56.5 mm^2	19.9 mm^2	160
Five Via Circuit Bottom Area	55.2 mm^2	49.9 mm^2	24.1 mm^2	160
Five Via Circuit Total Area	114.2 mm^2	111.1 mm^2	36.1 mm^2	160
Ten Via Circuit Top Area	105.5 mm^2	94.2 mm^2	37.7 mm^2	160
Ten Via Circuit Bottom Area	85.0 mm^2	75.0 mm^2	24.1 mm^2	160
Ten Via Circuit Total Area	190.5 mm^2	171.1 mm^2	70.2 mm^2	160

4.6.4 Physical Properties Summary

Physical properties results have shown that the failure location occurred 99.375% on the trace between the vias and pads on all circuit types in both experimentations, indicating that the quantity of vias has no direct impact on the failure location. There was a noticeable difference in how the physical properties changed as the circuits were headed towards failure, with the ten via showing the greatest changes with the surrounding dielectric bubbling around the vias due to having more heat dissipate into it, indicating it was at the boiling point. Furthermore, with the greater temperature in the dielectric leads to a more violent failure of the circuit resulting in a greater area of destruction around the circuit.

Chapter 5

Conclusion and Recommendations

5.1 Conclusion

In this dissertation, an investigation and analysis were conducted to meet the aim *to investigate the design rule of via minimization in PCB manufacturing by observing the impacts that the quantity of vias has on the reliability of PCB circuits* through maximum current and thermal experimentation on PCBs with circuits that contained either one, five or ten plated through-hole vias. The result of the experimentations shows that the quantity of vias had limited beneficial impacts on the reliability of PCB circuits, with the ten via circuits being able to maintain current at high temperatures and the temperature difference between the ten and five via circuits at the lower current levels being negligible. Overall, the experimentations showed the quantity of vias impact on the PCB circuits where overall detrimental, with the ten via circuits having the lowest maximum current, a more destructive failure that resulted in an increased area of damage around the circuit, and the one via circuits having the lowest temperatures out of the three types. Concluding the dissertation, that the increased quantity of via had an overall detrimental impact on PCB circuits, validating the design rule of via minimization.

5.2 Recommendations

With this dissertation concluding that the quantity of vias has an overall detrimental impact on the reliability of PCB circuits, validating the design rule of via minimisation and meeting the objective to provide recommendations in PCB design by using vias based on the results. Going forward, the recommendations with PCB design and the use of vias when designing for DC circuits are:

1. Follow the design rule of Via minimisation and keep the number of vias to a minimum, if capable, design to have zero vias as part of the circuit.
2. If the use of multiple vias cannot be avoided, maximise the distance between each via to reduce the impact of via fields accumulating between the vias.

3. Another recommendation is to design the vias with inside and outside diameters greater than the width of the trace they are interconnecting with; this is to increase their cross-sectional area reducing the amount of resistance the via are adding to the circuit.
4. The final recommendation with the use of via is to design the circuits to have the maximum amount of free FR-4 dielectric surrounding the vias, to allow the area for the heat to dissipate.

5.3 Contribution

The main contribution of this dissertation is that by validating the design rule of via minimisation, PCBs can be more efficiently designed to improve reliability, reducing failure of PCBs, which will reduce future e-waste; furthermore, it adds confidence to engineers in designing PCBs for manufacturing to use the design rule. Another contribution is through the literature review, it was identified that there is limited current research in the field of vias and PCB design, opening multiple avenues for future engineering research to optimise PCB design and opening multiple avenues for future engineering research to optimise PCB design. The final contribution of this dissertation is that it adds further knowledge about vias and their interactions in PCB circuits.

5.4 Further work

As was identified in the literature review, the reliability of a PCB circuit due to the quantity of vias is an under-research area, and there is room for further research as follows:

- Experimentation on different quantities of vias, as in this dissertation results, showed that between five and ten vias, there is a change in the impact on reliability, and there is room for greater quantities above ten vias.
- Comparison between different manufacturers to investigate if the manufacturing process impacts the reliability of PCB circuits regarding vias.
- Experimentation comparing the reliability based on quantities of vias through different dimensions of the interconnections; these include trace widths, lengths, and thickness via outer and inner diameter. PCB circuit design is as varied as applications that require a PCB.

- Investigation into the quantity of vias impact on PCBs with having conductive layers greater than two. As PCBs become more condensed with components, more layers are used in design.
- Investigation into the quantity of vias impact on PCBs with a type other than plated through holes, including blind, buried, tenting, micro vias, and filled vias (silicon). With PCB design, different types of vias are used depending on the application in need.
- Investigation into how the resistance changes due to the current level and temperature based on the quantity of vias.
- Investigation into the impact the quantities of vias have on circuits that use different electrical signals other than direct current; these include low and high frequency, analogue or digital signals, high power, and alternate current. PCBs can carry different electrical signals, and each can be impacted differently.
- Investigation into the quantity of vias that one circuit has on nearby other circuits; they could contain direct current or other signal types and components. PCBs are typically not empty and contain components, circuits that carry other signals, testing points, and interconnections external to the PCB.

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Appendix A

Project Specification

For: Christopher Preddy

Topic: An Investigation into the Failure Characteristics of Different Quantities of Plated Through Hole Vias (Version 1.0, 14 February 2024)

An Investigation into the Impact Different Quantities of Vias Have on the Reliability of PCB Circuits (Version 2.1, 26 August 2024)

Supervisor: Dr Jason Brown

Sponsorship: UniSQ School of Engineering

Project Aim: To investigate the design rule of via minimization in PCB manufacturing and its impacts on the reliability of PCB circuits.

Program: Version 1.0, 14 February 2024

This program specification was first established at the beginning of the academic year 2024

- **Weeks 1-4: Specification, Project plan, administration**
  - Research background information and, write a report, develop a title for the project.
  - State objectives and expectations of the project.
  - Develop a detailed plan and the resources required.
  - Organise access to the engineering laboratories at the Springfield campus.
  - Organise meetings with the supervisor.
  - Acquire resources that have not already been acquired.
- **Weeks 1-6: Design and manufacture experimentation PCBs**
  - Design circuits that will test a range of via quantities.
  - Have the PCBs manufactured and delivered for experimentation.
  - Inspect PCBs upon delivery for defects, and the circuit will be marked.
- **Weeks 3-4: Develop an initial methodology and do a risk management plan (RMB)**
  - Write up an initial methodology of expected testing to present to the supervisor to be able to start testing in the first trimester.

    - Develop a risk management plan for testing at university engineering laboratories and at home.
- **Weeks 5-6: Initial testing**
    - Conduct basic testing to ensure equipment works.
    - Decide on a third circuit containing either 5 or 15 vias.
    - Determine if the dimensions of the vias and trace need to be adjusted.
- **Weeks 4-18: Literature Review**
    - Conduct an in-depth literature review into the impacts of multiple Via on a PCB circuit, focusing on current limitations and temperature.
    - Finalize the research design and methodology.
- **Weeks 6-14: One via experimentation**
    - Conduct over current testing on circuits that contain one via.
    - Record maximum current, thermal images, and note physical location.
- **Weeks 10-18 Formalize methodology.**
    - Formalizing the methodology started developing in weeks 3-4 to prepare for the assessment and the final dissertation.
- **Weeks 14-22: Ten vias experimentation**
    - Conduct over current testing on circuits that contain ten via.
    - Record maximum current, thermal images, and note physical location.
- **Weeks 22-30: Five or fifteen vias experimentation**
    - Conduct over-current testing on circuits that either contain 5 or 15 vias.
    - Record maximum current, thermal images, and note physical location.
- **Weeks 9-32: Statistical Analysis and Physical inspection**
    - Compare statistical results between the results, looking at the mean, median and standard deviation.
    - Inspect the circuits to identify where the failure has occurred and key locations, such as vias, trace, dielectric, and connection pads.
- **Weeks 3-34: Write a draft dissertation.**
    - Write the dissertation of the project and build it up over the project duration. Assessment is due in week 34.
- **Weeks 36-39: Prepare and present findings.**
    - Prepare a presentation to present the findings to peers at the engineering conference in week 39 conducted by UniSQ.
- **Weeks 1-40: Reflection.**
    - Take notes throughout the project on aspects such as difficulties, what was learnt, and areas that could be improved.
    - Finalize reflection into a report during weeks 38-40 for Assessment due week 40.
- **Weeks 34-43: Dissertation Completion.**
    - Review the draft dissertation result, correct, and finalize the dissertation for project completion. Assessment is due week 43.

Below are optional plans; these depend on the speed at which the conducting of the testing on the circuits and other commitments takes; below are the major changes:

- **Weeks 6-11: One via dimension 1 circuit experimentation**
    - Conduct over current testing on circuits that contain one via.
    - Record maximum current thermal images and note the physical location.

- **Weeks 8-11: Design and manufactured dimension two experimentation PCBs**
    - Copy the original PCB design and modify the dimensions on the Vias.
    - Have the same manufacturer produce the PCBs.
- **Weeks 10-15: Ten vias of dimension 1 circuit experimentation**
    - Conduct over-current testing on circuits that contain ten vias.
    - Record maximum current, thermal images, and note physical location.
- **Weeks 14-19: Five or fifteen via dimension 1 circuit experimentation**
    - Conduct over-current testing on circuits that contain 5 or 15 vias.
    - Record maximum current, thermal images, and note physical location.
- **Weeks 18-23: One via dimension 2 circuit experimentation**
    - Conduct over current testing on circuits that contain one via.
    - Record maximum current, thermal images, and note physical location.
- **Weeks 22-27: Ten vias of dimension 2 circuit experimentation**
    - Conduct over-current testing on circuits that contain ten vias.
    - Record maximum current, thermal images, and note physical location.
- **Weeks 26-31: Five or fifteen via dimension 2 circuit experimentation**
    - Conduct over-current testing on circuits that contain 5 or 15 vias.
    - Record maximum current, thermal images, and note physical location.

Version 2.0, 3 April 2024

This version was revised when it was decided to split the experiment between maximum current and thermal properties. The changes are below.

- **Weeks 5-6: Initial testing maximum current**
    - Conduct basic testing to ensure equipment works.
    - Decide on a third circuit containing either 5 or 15 vias.
    - Determine what methodology would be best to find the maximum current
    - Run practice experiments to confirm best-of-fit methodology
- **Weeks 6-16: Conducted Maximum current experiments**
    - Conduct experiments on the one, five and ten via circuits
    - Record maximum current results in Excel
    - Video record experiment to observe failure after testing is completed
- **Weeks 13-14: Initial Thermal testing**
    - Collect the FLIR i5 thermal camera from the technical staff at the Springfield campus.
    - Determine methodologies to use to address objectives.
    - Test different mythologies to ensure the best fit for the experiment.
- **Weeks 14-16: Conducted thermal properties experiments**
    - Conduct experiments on the one, five and ten via circuits
    - Capture thermal images at different current levels
    - Capture physical photos at different current levels
    - Record the temperature at each different current level in Excel
- **Weeks 9-32: Statistical Analysis and Physical inspection**
    - Compare results statistically for maximum current, looking at the mean, median and standard deviation

        - Compare results statistically for temperate at different current levels, looking at the mean, median and standard deviation
        - Inspect the circuits to identify where the failure has occurred and key locations, such as vias, trace, dielectric, and connection pads.
        - Inspect the thermal photos to see any noticeable differences in thermal properties.
        - Inspect physical photos to see if there are physical differences between circuits at different current levels.

All previous optional plans were changed to the one below:

- **Weeks 17-22: Conducted further Maximum current and thermal experiments**
    - If time permits, conduct further experiments to add more data to the results
    - Time allowed for any errors that occurred during previous experiment time slots

Appendix B

Project Time Tables

Figures B1 and B2 below are the timetables used for the project. Figure B2: is the revised timetable that came about when the initial maximum current testing was conducted, and it was decided to separate the maximum current and thermal experiment due to the unknown timeframe that the FLIR i5 camera would be available for the project.

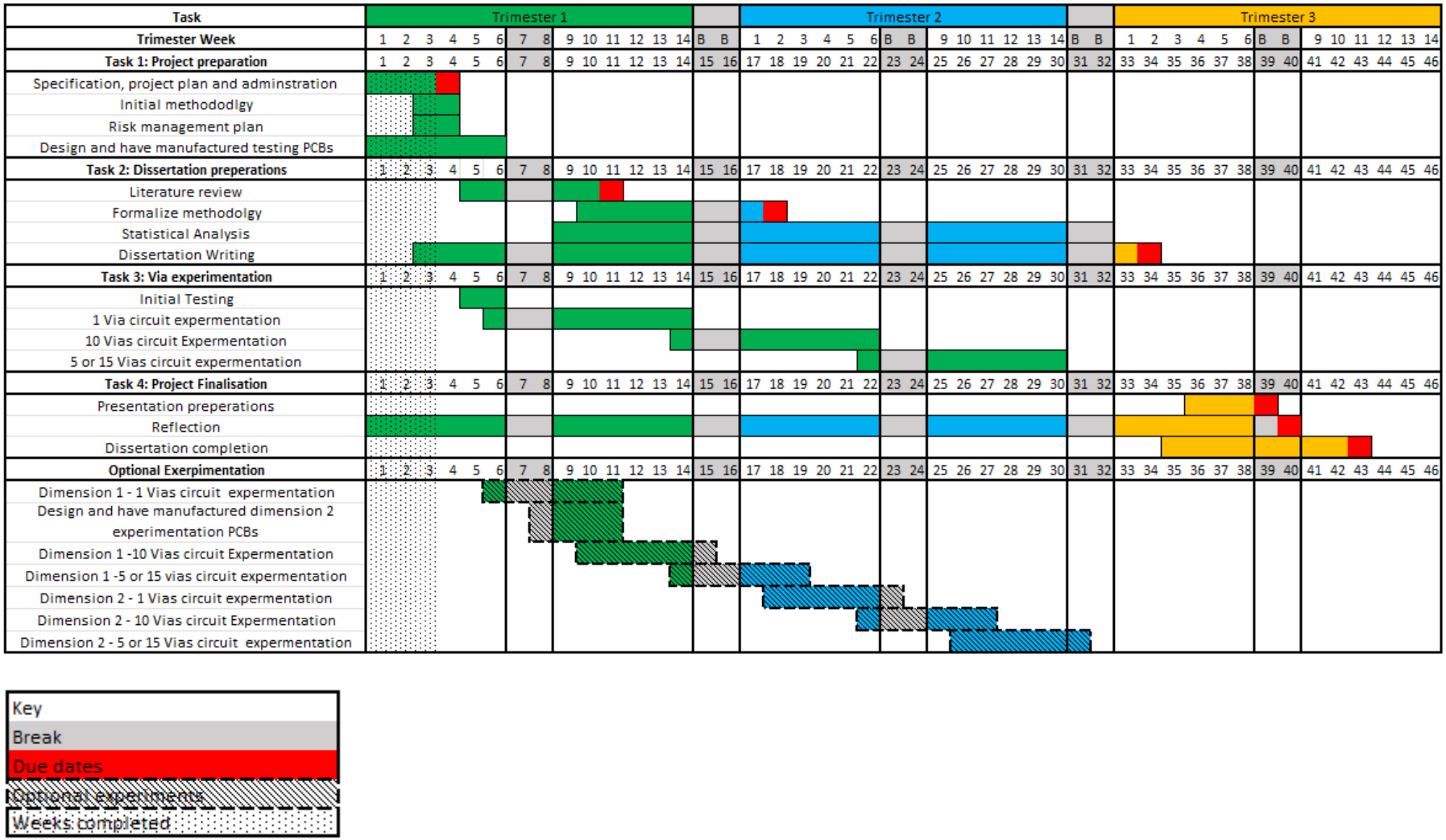


Figure B1: Gantt Chart for the Project Version 1.0, 14 February 2024.

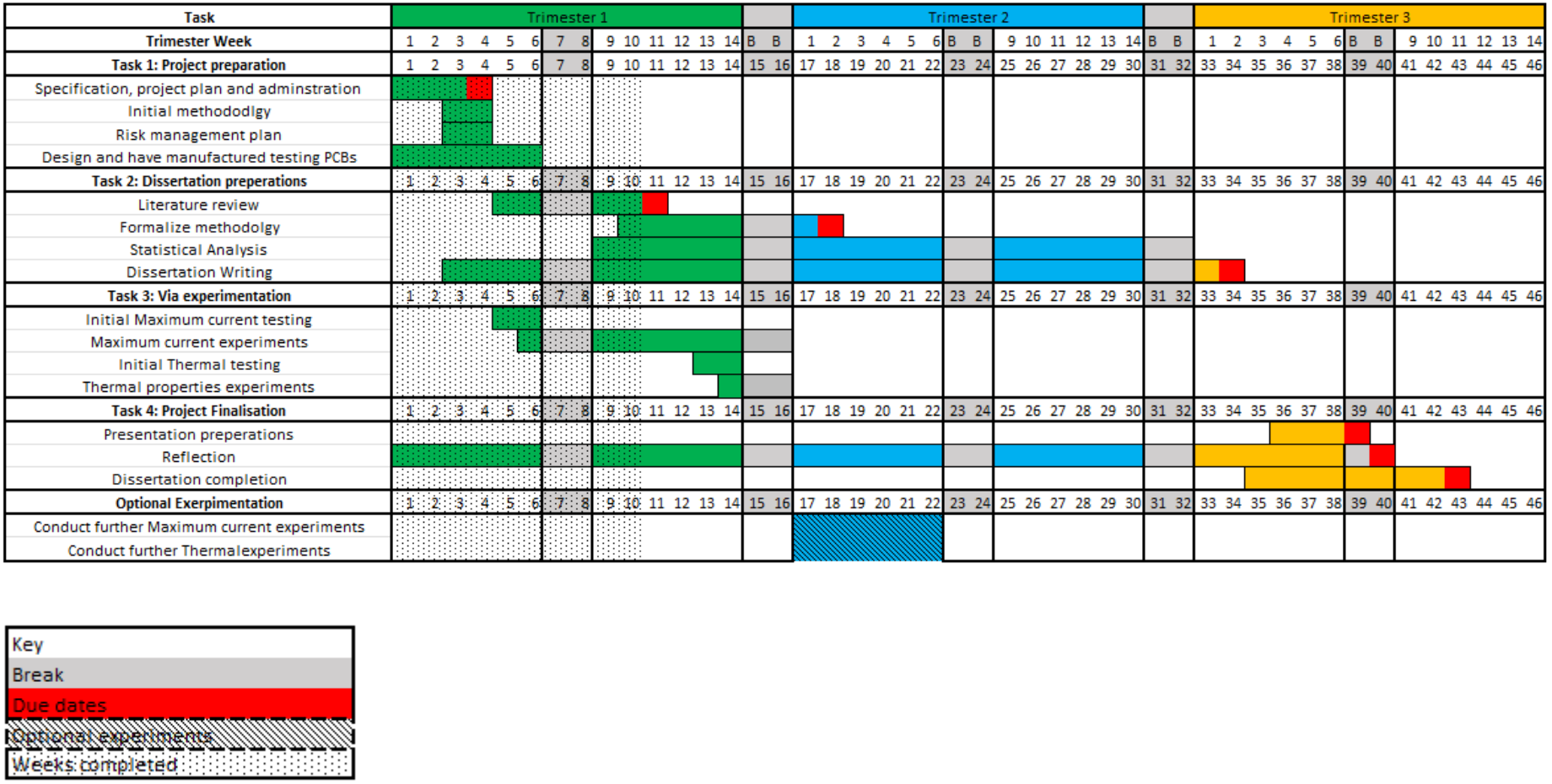
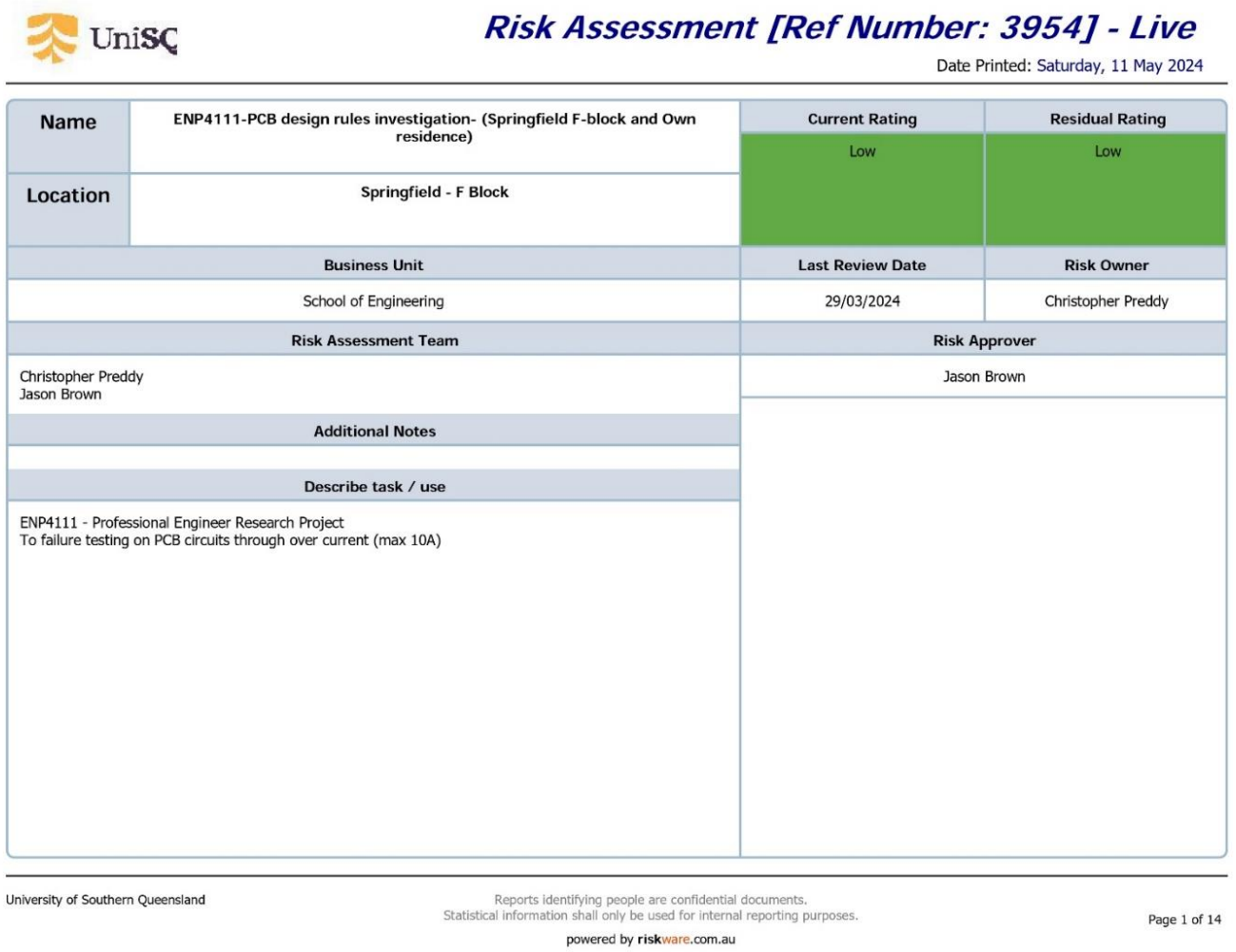


Figure B2: Gantt Chart for the Project Version 2.0, 3 April 2024.

Appendix C

Risk Management Plan

Below, in Figure C1-C14 are the screenshots of the risk management plan required for this dissertation. The major risks identified were working with live power with currents reaching up to 10A, fire due to the circuits and the FR-4 dielectric igniting, and fumes produced; the minor risks involved cutting wires, ergonomics, and cleaning products. The risk management plan was implemented for UniSQ engineering laboratory access in F-block at the Springfield campus and the private property.



UniSC

Risk Assessment [Ref Number: 3954] - Live

Date Printed: Saturday, 11 May 2024

Name	ENP4111-PCB design rules investigation- (Springfield F-block and Own residence)	Current Rating	Residual Rating
Location	Springfield - F Block	Low	Low

Business Unit	Last Review Date	Risk Owner
School of Engineering	29/03/2024	Christopher Preddy

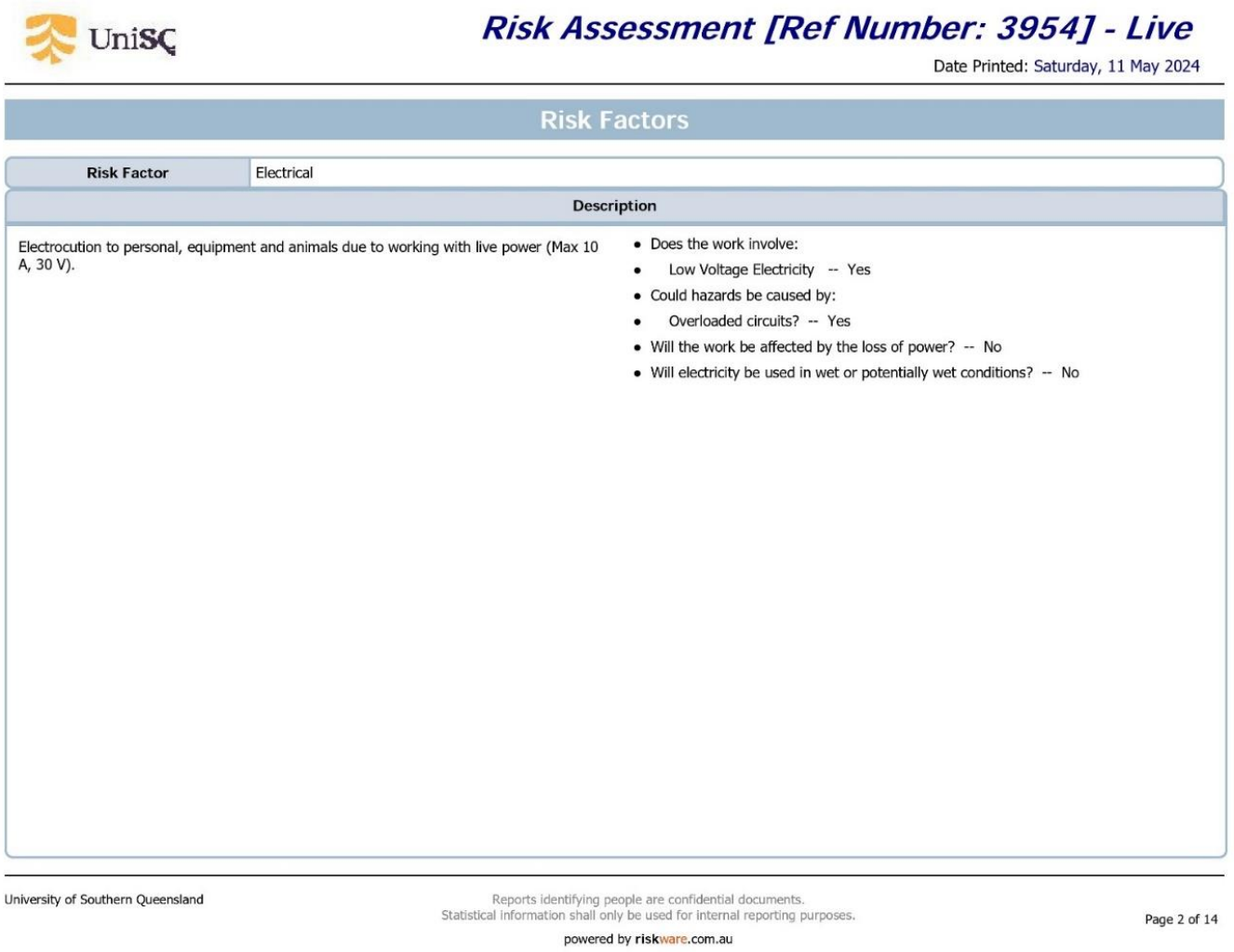
Risk Assessment Team	Risk Approver
Christopher Preddy Jason Brown	Jason Brown

Additional Notes

Describe task / use

ENP4111 - Professional Engineer Research Project
To failure testing on PCB circuits through over current (max 10A)

Figure C1: Image of page 1 of 14 of the risk assessment for dissertation testing.



UniSC

Risk Assessment [Ref Number: 3954] - Live

Date Printed: Saturday, 11 May 2024

Risk Factors

Risk Factor	Electrical

Description

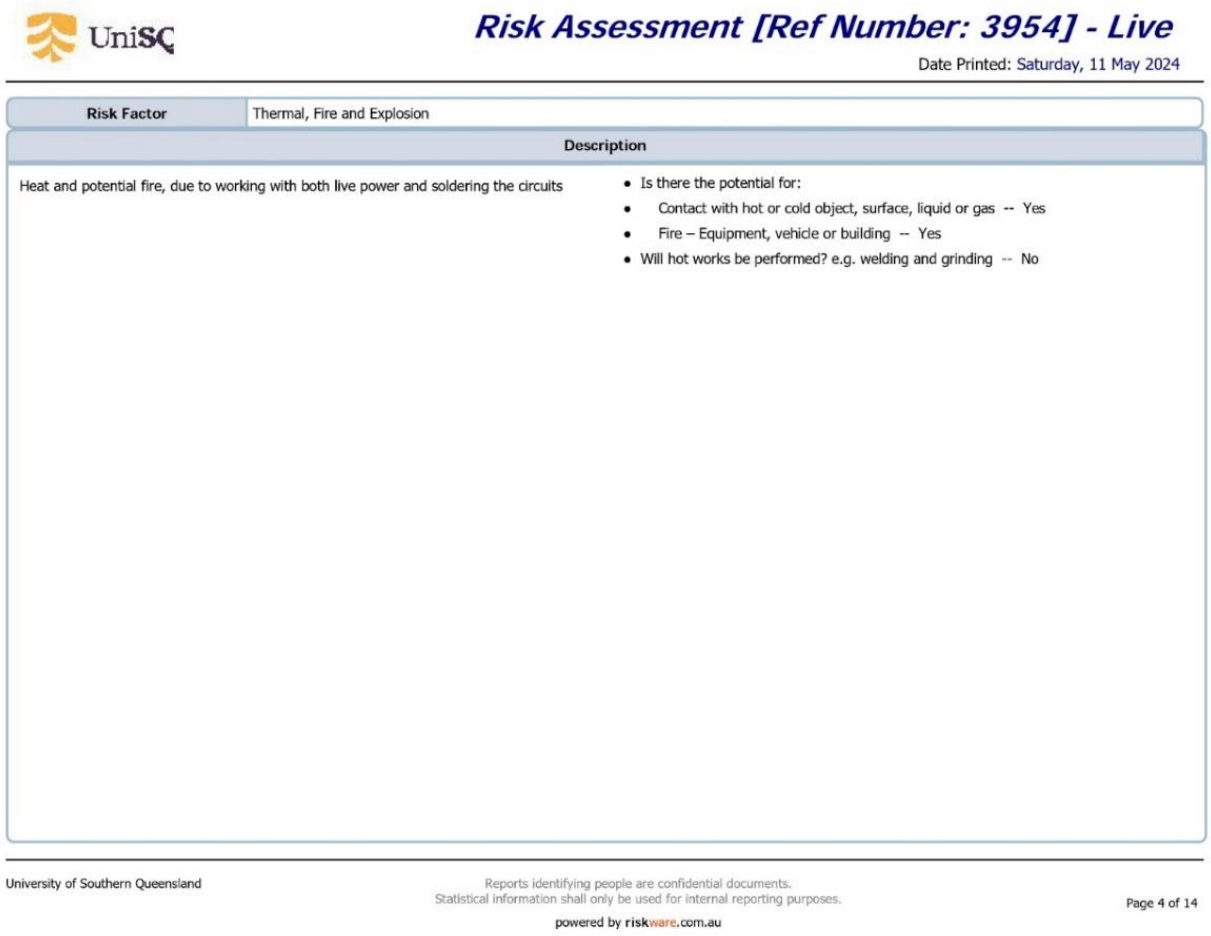
Electrocution to personal, equipment and animals due to working with live power (Max 10 A, 30 V).

- Does the work involve:
- Low Voltage Electricity -- Yes
- Could hazards be caused by:
- Overloaded circuits? -- Yes
- Will the work be affected by the loss of power? -- No
- Will electricity be used in wet or potentially wet conditions? -- No

Figure C2: Image of page 2 of 14 of the risk assessment for dissertation testing.

Low	Low
Existing Controls	**Proposed Controls**
• 5 - Administration: Student has a Cert. IV in electronic telecommunication and has 7.5 years of industry experience working with live equipment. Know emergency contact numbers. Equipment will be used in accordance with their technical manuals. During testing, the only contact will be with the power supply controls. Zero contact with the circuit once the power has been applied. Restrictive access to the testing location to qualified personal. Additional person will be notify that testing will be conducted on the days(F-block technical staff, supervisor) • 4 - Engineering: 30V is insufficient to cause a serious electrocution risk (due to the fact the resistance of the human body is of the order of 1MΩ) Work in area that has over current protection. Workspace has switches to isolate power. Test equipment being used can easily be turned off. • 1 - Elimination: Zero Pets At students residence	

Figure C3: Image of page 3 of 14 of the risk assessment for dissertation testing.



UniSC

Risk Assessment [Ref Number: 3954] - Live

Date Printed: Saturday, 11 May 2024

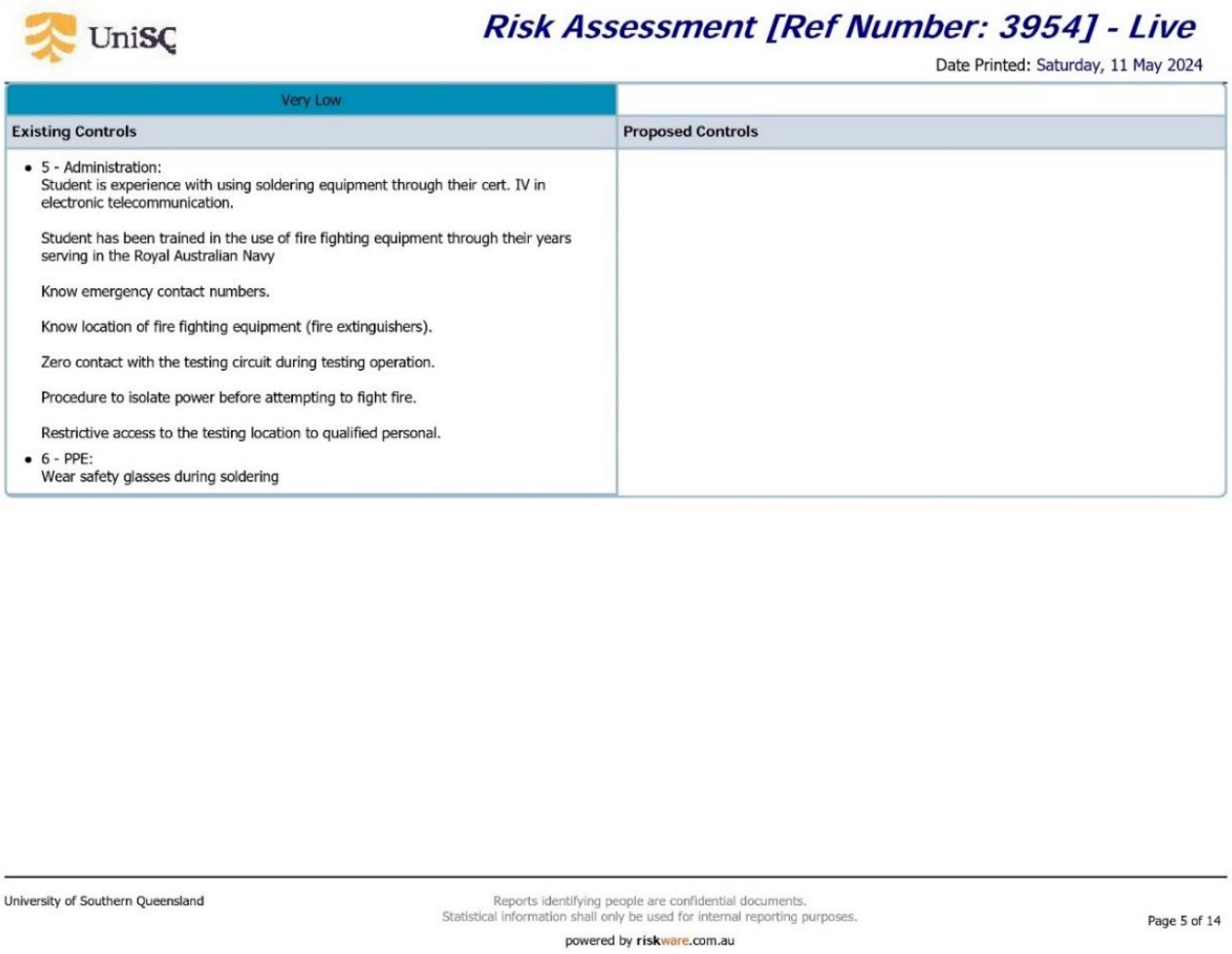
Risk Factor	Thermal, Fire and Explosion

Description

Heat and potential fire, due to working with both live power and soldering the circuits

- Is there the potential for:
- Contact with hot or cold object, surface, liquid or gas -- Yes
- Fire – Equipment, vehicle or building -- Yes
- Will hot works be performed? e.g. welding and grinding -- No

Figure C4: Image of page 4 of 14 of the risk assessment for dissertation testing.



UniSC

Risk Assessment [Ref Number: 3954] - Live

Date Printed: Saturday, 11 May 2024

Very Low	
Existing Controls	**Proposed Controls**
• 5 - Administration: Student is experience with using soldering equipment through their cert. IV in electronic telecommunication. Student has been trained in the use of fire fighting equipment through their years serving in the Royal Australian Navy Know emergency contact numbers. Know location of fire fighting equipment (fire extinguishers). Zero contact with the testing circuit during testing operation. Procedure to isolate power before attempting to fight fire. Restrictive access to the testing location to qualified personal. • 6 - PPE: Wear safety glasses during soldering	

Figure C5: Image of page 5 of 14 of the risk assessment for dissertation testing.

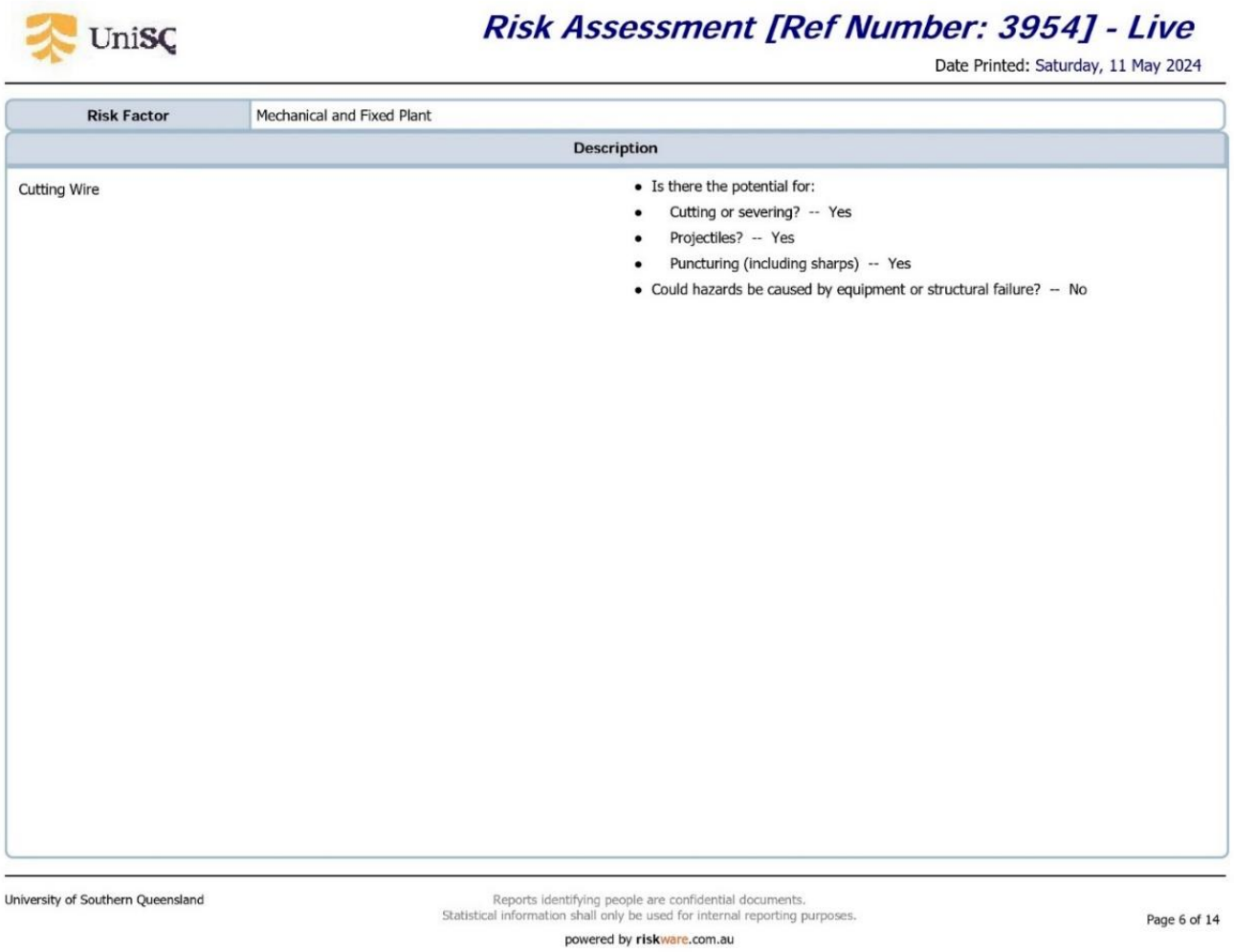


Figure C6: Image of page 5 of 14 of the risk assessment for dissertation testing.

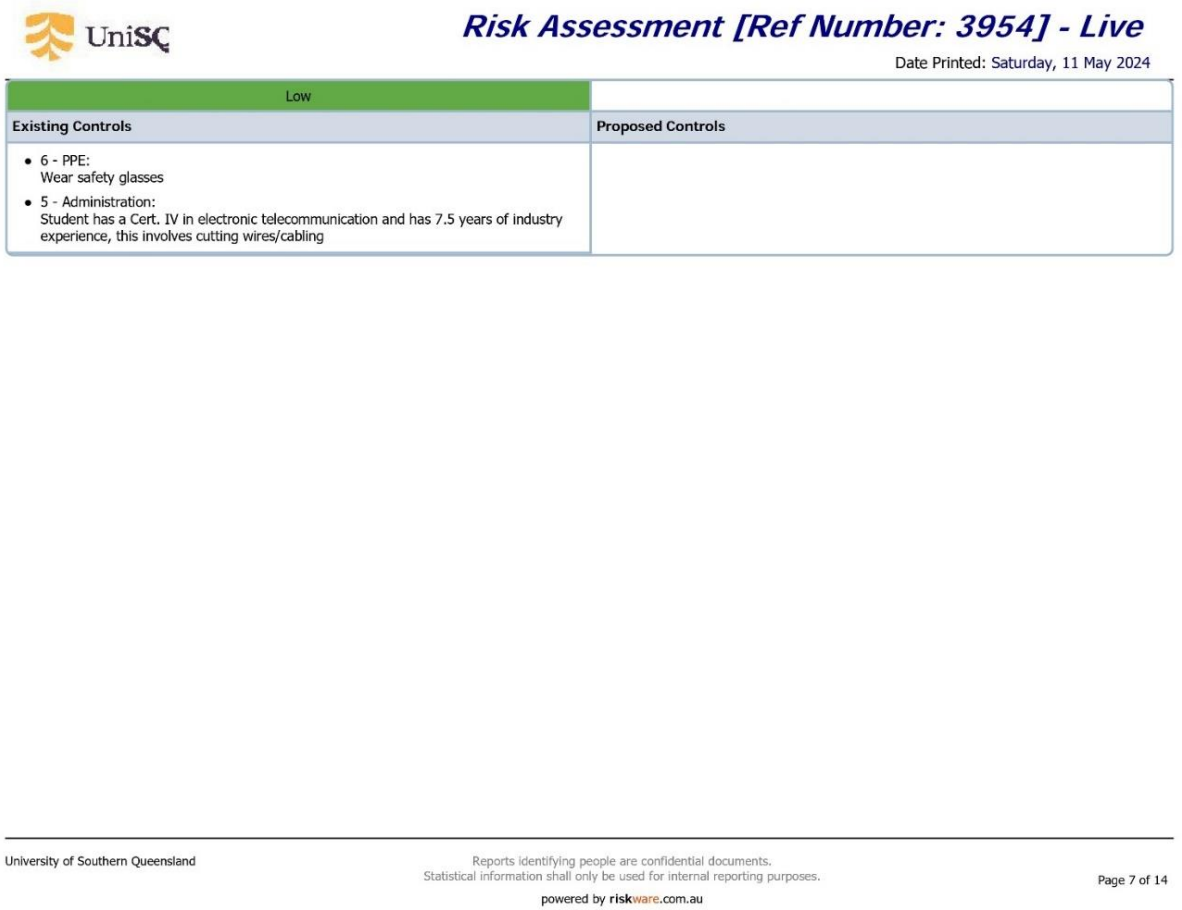
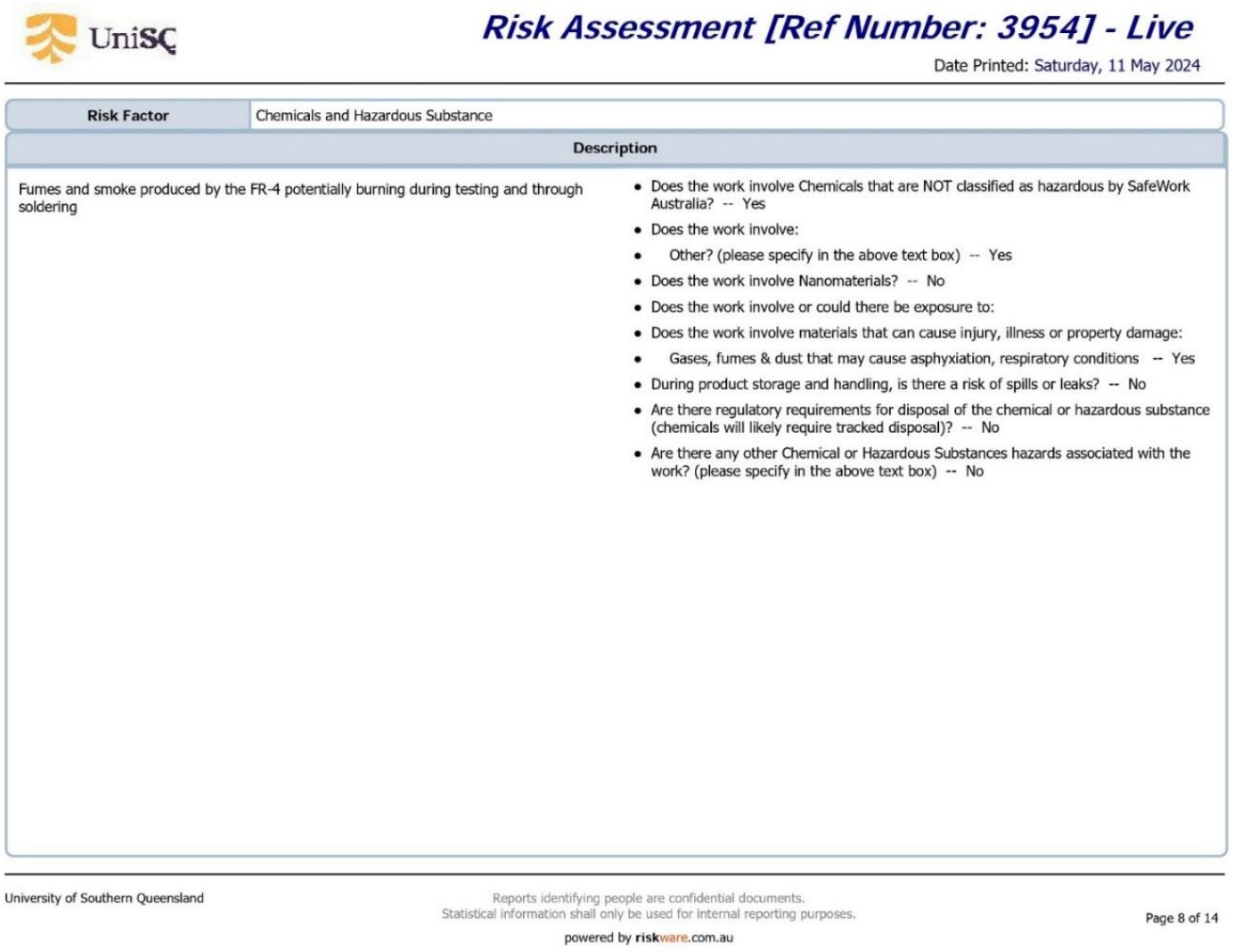


Figure C7: Image of page 7 of 14 of the risk assessment for dissertation testing.



UniSQ

Risk Assessment [Ref Number: 3954] - Live

Date Printed: Saturday, 11 May 2024

Risk Factor	Chemicals and Hazardous Substance

Description

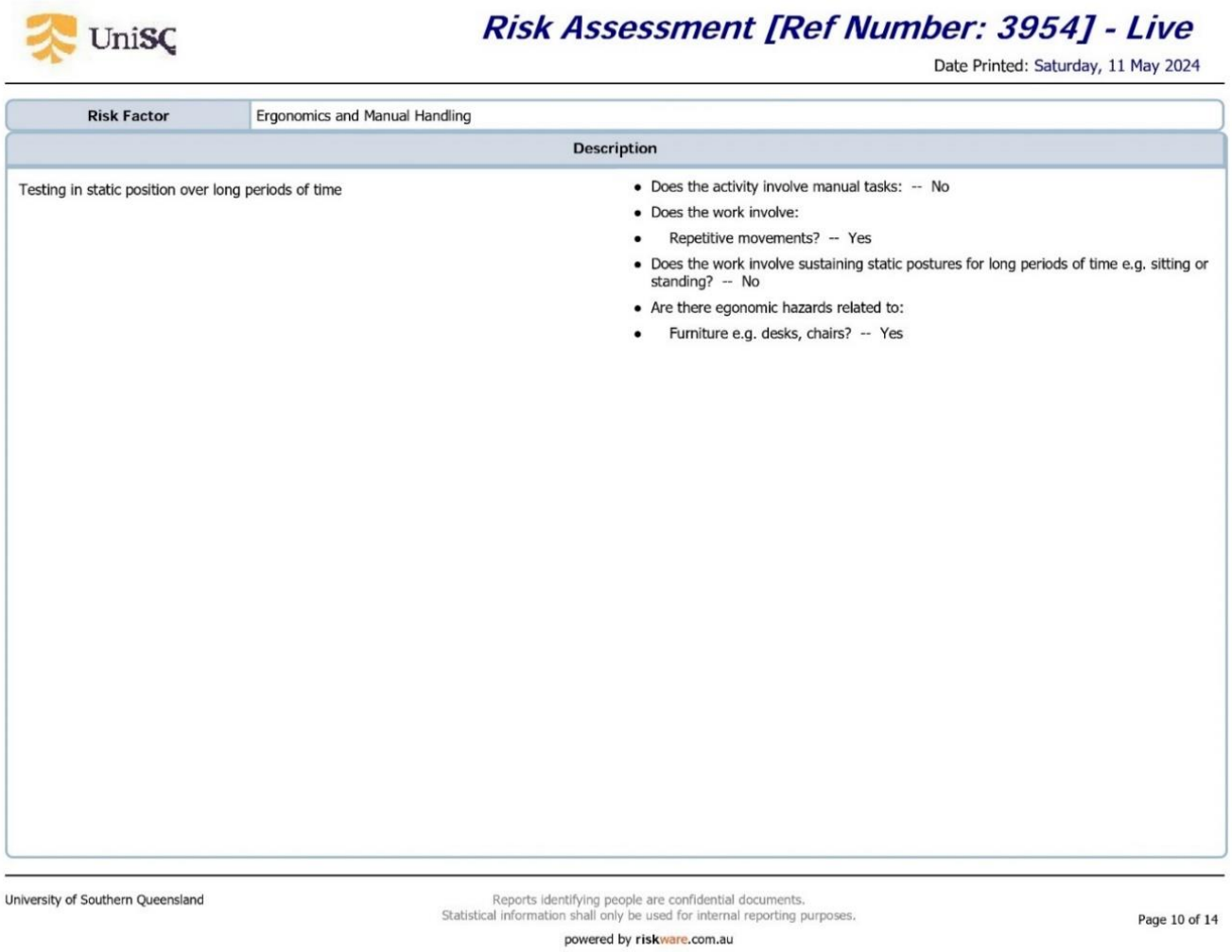
Fumes and smoke produced by the FR-4 potentially burning during testing and through soldering

- Does the work involve Chemicals that are NOT classified as hazardous by SafeWork Australia? -- Yes
- Does the work involve:
- Other? (please specify in the above text box) -- Yes
- Does the work involve Nanomaterials? -- No
- Does the work involve or could there be exposure to:
- Does the work involve materials that can cause injury, illness or property damage:
- Gases, fumes & dust that may cause asphyxiation, respiratory conditions -- Yes
- During product storage and handling, is there a risk of spills or leaks? -- No
- Are there regulatory requirements for disposal of the chemical or hazardous substance (chemicals will likely require tracked disposal)? -- No
- Are there any other Chemical or Hazardous Substances hazards associated with the work? (please specify in the above text box) -- No

Figure C8: Image of page 8 of 14 of the risk assessment for dissertation testing.

Low	
Existing Controls	**Proposed Controls**
• 4 - Engineering: use of installed fume extractors in the engineering laboratory or a use portable fume extractor. Work in well ventilated work space. • 5 - Administration: Do not work directly above the tested circuit.	

Figure C9: Image of page 9 of 14 of the risk assessment for dissertation testing.



UniSC

Risk Assessment [Ref Number: 3954] - Live

Date Printed: Saturday, 11 May 2024

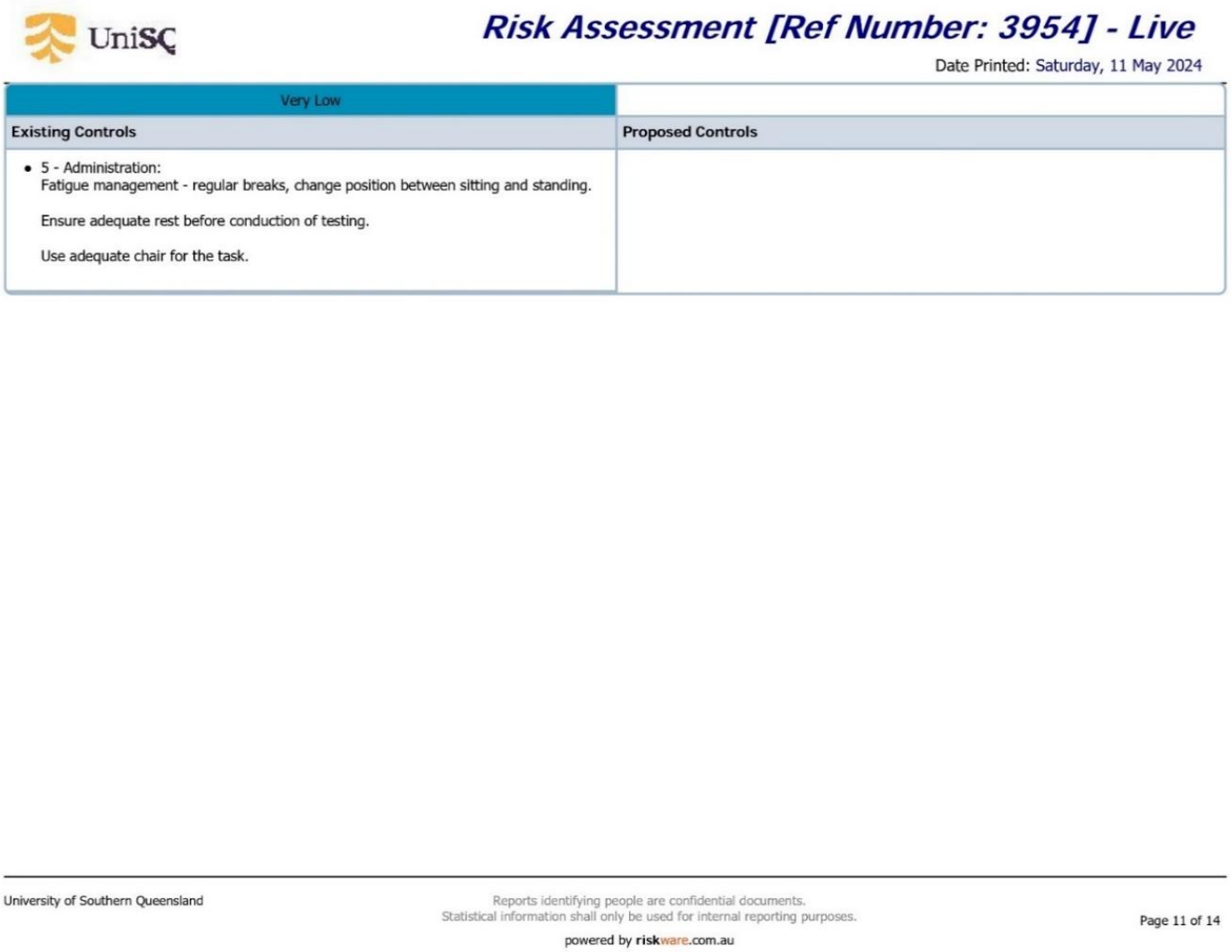
Risk Factor	Ergonomics and Manual Handling

Description

Testing in static position over long periods of time

- Does the activity involve manual tasks: -- No
- Does the work involve:
- Repetitive movements? -- Yes
- Does the work involve sustaining static postures for long periods of time e.g. sitting or standing? -- No
- Are there egonomic hazards related to:
- Furniture e.g. desks, chairs? -- Yes

Figure C10: Image of page 10 of 14 of the risk assessment for dissertation testing.



UniSC

Risk Assessment [Ref Number: 3954] - Live

Date Printed: Saturday, 11 May 2024

Very Low	
Existing Controls	**Proposed Controls**
• 5 - Administration: Fatigue management - regular breaks, change position between sitting and standing. Ensure adequate rest before conduction of testing. Use adequate chair for the task.	

University of Southern Queensland

Reports identifying people are confidential documents.
Statistical information shall only be used for internal reporting purposes.

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Page 11 of 14

Figure C11: Image of page 11 of 14 of the risk assessment for dissertation testing.

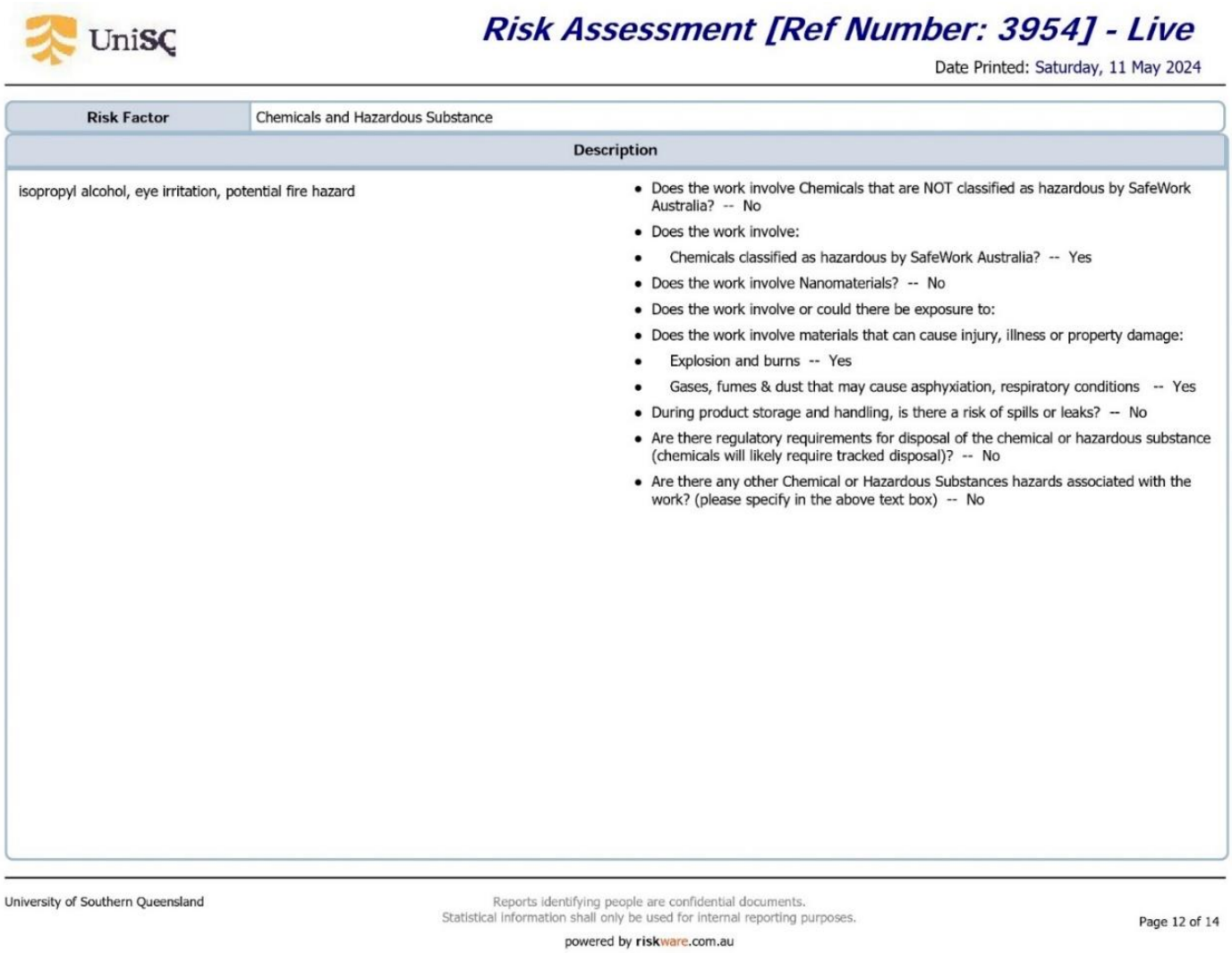
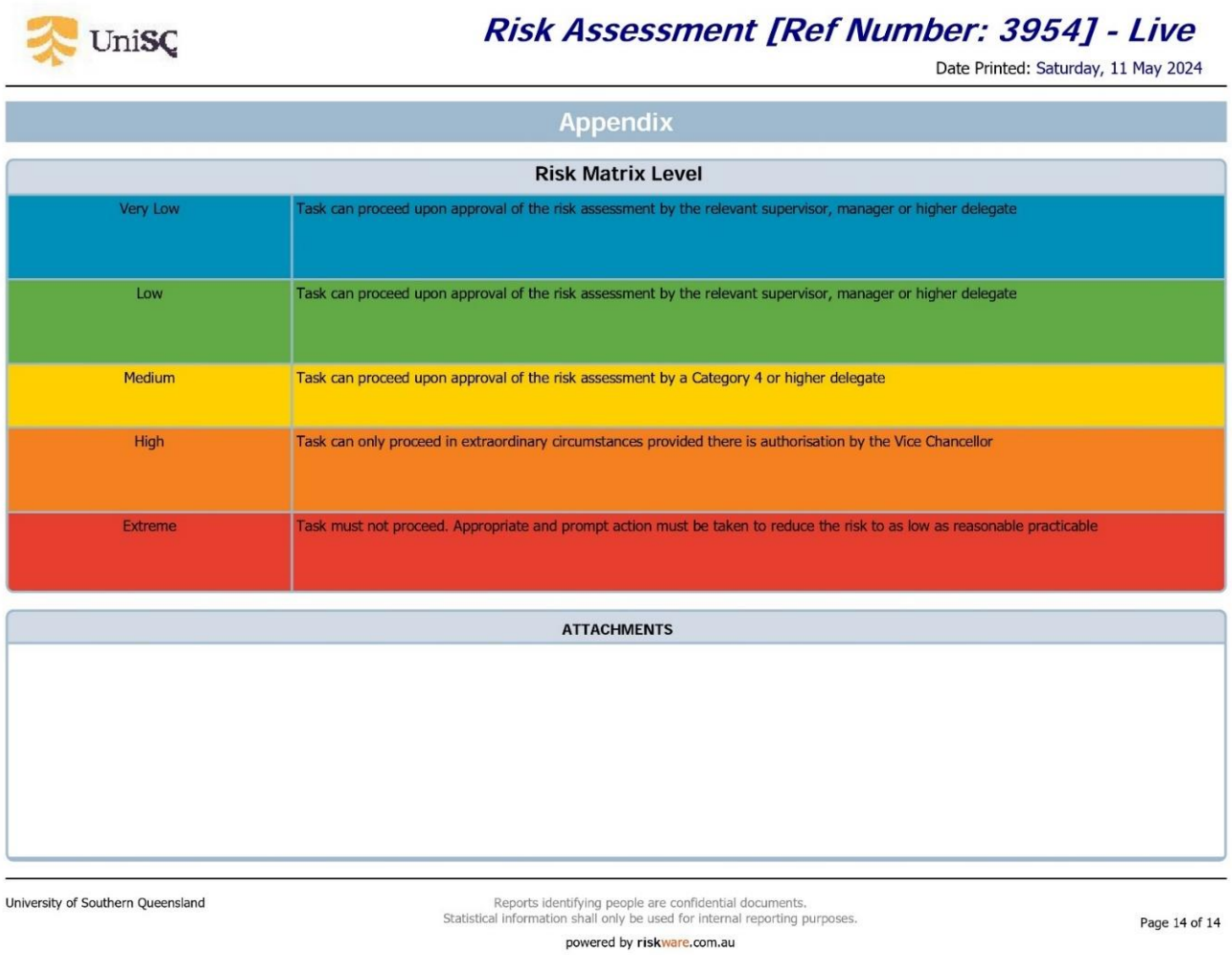


Figure C12: Image of page 12 of 14 of the risk assessment for dissertation testing.

Very Low	
Existing Controls	**Proposed Controls**
• 5 - Administration: - Use along side safety data sheet - Keep away from naked flames - Wait for a couple of minutes after use before applying any power to the experiment, to ensure it has evaporated. • 6 - PPE: - Use eye protection - Use gloves • 4 - Engineering: - Keep in a sealed container when not in use - Work in a well ventilated space	

Figure C13: Image of page 13 of 14 of the risk assessment for dissertation testing.



UniSC

Risk Assessment [Ref Number: 3954] - Live

Date Printed: Saturday, 11 May 2024

Appendix

Risk Matrix Level	
Very Low	Task can proceed upon approval of the risk assessment by the relevant supervisor, manager or higher delegate
Low	Task can proceed upon approval of the risk assessment by the relevant supervisor, manager or higher delegate
Medium	Task can proceed upon approval of the risk assessment by a Category 4 or higher delegate
High	Task can only proceed in extraordinary circumstances provided there is authorisation by the Vice Chancellor
Extreme	Task must not proceed. Appropriate and prompt action must be taken to reduce the risk to as low as reasonable practicable

ATTACHMENTS

Figure C14: Image of page 14 of 14 of the risk assessment for dissertation testing.

Appendix D

Ethical Clearance

There are no Ethical Clearances applicable to this project.

Appendix E

List of Equipment Used

Below in Table E1 is the complete list of equipment used in this dissertation; it contains the name and quantity; it also includes the key parameters, for example, maximum current it can read and comment, which include who provided access to the equipment such as UniSQ or the datasheet/manual for the equipment.

Table E1: List of Equipment Used.

Item	Qty.	Key parameter	Comment
Laptop with Microsoft Windows	1	Nil	
PC with Microsoft Windows	1	Nil	
Microsoft Word	1	Nil	Provide by UniSQ
Microsoft Excel	1	Nil	Provided by UniSQ
PCBs	30 (min)	Nil	Manufactured by JLCPCB
EasyEDA program	1	Nil	
High power resistor	3	100 W 3.3 Ω	(ARCOL, 2008)
IPA	3	99.8% pure 250 mL	(Chemtools, 2023)

UT61E+ Software	1	Nil	It comes with the UT61E+ Multimeter (UNI-T, n.d.)
Jesverty SPS-3010N Power supply	1	0 - 30 V 0 - 10 A 300 W	(Jesverty, n.d.)
UT61E+ Multimeter	1	20 A ± (1.2%+50) (max range) 10 A, 240 V (Overload protection)	(UNI-T, n.d.)
FLIR i5 Thermal camera	1	+270 °C (Max)	(FLIR, 2011) Provided by UniSQ
Protech Infrared Thermometer	1	-50 °C (Minimum) 500 °C (Maximum)	(Protech, n.d.)
Magnifying Glass	1	Nil	
Noevsbig Fume Extractor	1	Nil	It uses carbon fibre sheets
Overhead Camera holder	1	Nil	
Helping hands soldering station	1	Nil	It has four alligator clips, a ring light, a magnifying glass
Ruler	1	20 cm	Plastic