University of Southern Queensland

Faculty of Engineering and Surveying

DESIGN AND IMPLEMENTATION OF A REMOTELY ACCESSIBLE INRUSH CURRENT TESTING PACKAGE FOR POWER (DISTRIBUTION) TRANSFORMERS

A dissertation submitted by

Glenn SPRINGALL

In fulfillment of the requirements of

Courses ENG4111 and 4112 Research Project

towards the degree of

Bachelor of Engineering (Electrical/Electronic) and Bachelor Science (Chemistry)

Submitted: October, 2008

ABSTRACT

Inrush current or surge current in Power (distribution) transformers has been known to exist since transformers were first designed and manufactured. Since that time, the phenomenon has been researched, modelled and factored into designs.

This project analyses the harmonics that exist within inrush current and also the techniques utilised in the managing of nuisance tripping caused by the high inrush current spikes. Additionally this project provides training and education tools for University Students. Primarily through a theoretical module and then complimented by a practical observation activity on a test rack suitable for remote access.

University of Southern Queensland
Faculty of Engineering and Surveying

ENG4111 Research Project Part 1 & ENG4112 Research Project Part 2

LIMITATIONS OF USE

The Council of the University of Southern Queensland, its Faculty of Engineering and Surveying, and the staff of the University of Southern Queensland, do not accept any responsibility for the truth, accuracy or completeness of material contained within or associated with this dissertation.

Persons using all or any part of this material do so at their own risk, and not at the risk of the Council of the University of Southern Queensland, its Faculty of Engineering and Surveying or the staff of the University of Southern Queensland.

This dissertation reports an educational exercise and has no purpose or validity beyond this exercise. The sole purpose of the course "Project and Dissertation" is to contribute to the overall education within the student’s chosen degree programme. This document, the associated hardware, software, drawings, and other material set out in the associated appendices should not be used for any other purpose: if they are so used, it is entirely at the risk of the user.

Professor Frank Bullen
Dean
Faculty of Engineering and Surveying

CERTIFICATION

I certify that the ideas, designs and experimental work, results, analyses and conclusions set out in this dissertation are entirely my own effort, except where otherwise indicated and acknowledged.

I further certify that the work is original and has not been previously submitted for assessment in any other course or institution, except where specifically stated.

Glenn William Springall
Student Number: 0050026015

____
Signature

____
Date

ACKNOWLEDGEMENTS

This research was carried out under the principle supervision of Dr Tony Ahfock. His support, knowledge and assistance have been vital in maintaining accurate and reliable research.

I would also like to acknowledge and thank Mr Don Gelhaar, USQ technical staff for laboratory assistance, Mr Vikram Kapadia for SCADA and PLC assistance.

Lastly I thank my wife, Melissa and the rest of my family for support and patience during this year and the prior years of study.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

GLOSSARY

USQ	University of Southern Queensland
PLC	Programmable Logic Controller
SCADA	Supervisory Control and Data Acquisition
EMF	Electromotive Force
CB	Circuit Breaker
CT	Current Transformer
OC	Overcurrent
REF	Restricted Earth Fault
LED	Light Emitting Diode
PPE	Personal Protective Equipment
SEF	Sensitive Earth Fault
AR	Autoreclose
FFT	Fast Fourier Transform

CHAPTER 1: INTRODUCTION

1.1 Justification for the Project

It is important that Electrical Engineers and Electrical Scientists alike, understand how and why a transformer works. It is important that they understand where losses occur, what those losses look like and what faults can occur inside and outside a transformer. This understanding is crucial if the industry is to see an increase in “SMART” transformers, to develop more energy efficient transformers, to increase transformer capacities and also to reduce the physical size of transformers.

This particular project investigates the inrush current phenomenon associated with the energisation of transformers, particularly power transformers. Much work has been completed in the past two hundred years to analyse transformers and their operation. This project aims to confirm those assumptions and findings through mathematical analysis of an inrush current test rack facility. Through this investigation the aims are to provide a resource for academics to use in creation of a well balanced, practical and theoretical course on either transformers or protection systems.

1.2 Dissertation Outline

The second chapter of this dissertation focuses on the background of inrush current. It explores the place that inrush current has in the power industry, particularly in transformer technologies and the effects and limitations on transformer designs. The chapter also covers some background information on how sequential switching and “SMART” relays are employed to combat nuisance tripping from high inrush currents.

Chapter three covers the methodologies used to achieve the project aims and objectives.

Chapter four is used to describe and outline the function that the differential relay plays in monitoring and combating nuisance tripping from inrush current. This chapter also details the appropriate way to set a differential relay to avoid inrush current tripping including second and fourth harmonic analysis.

Chapter five details the mathematics underpinning inrush current. Inrush current is analysed from the three phase example to determine the levels harmonic present using MATLAB.

The sixth chapter focuses on the teaching module of inrush current. This includes a theoretical component, a mathematical analysis component, a relay setting component, a practical component and then concluded by review questions.

Chapter seven outlines what works could be undertaken in the future that associate with this project. Details of the cost and benefit of conducting these works are also mentioned.

Finally this dissertation is concluded by a chapter outlining the summary of the achievements from this project and the conclusions made from conducting the project.

CHAPTER 2: LITERATURE REVIEW

2.1 Overview of Inrush Current

The problems associated with inrush current and the possible solutions and management of the high currents have been available for many years. It is very well known that the cause of inrush current is due to a combination of magnetic flux and part cycle voltage.

Figure 1 shows a simple transformer diagram of the primary windings (ie no load). In the diagram, v represents the voltage of EMF of the windings, i represents the primary side current, N represents the number of turns (of the windings) and x is a switch.

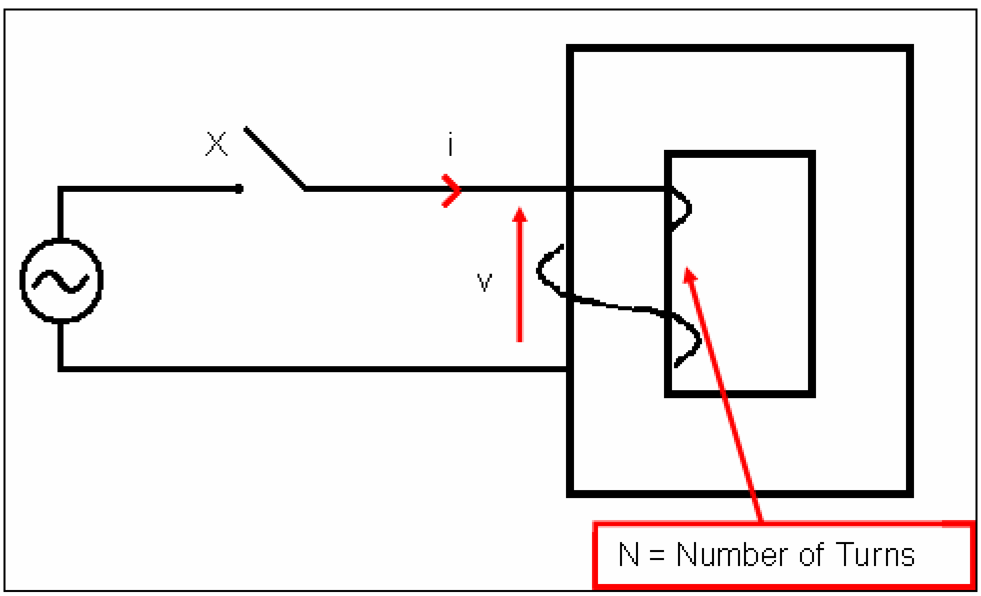

Figure 1 - Transformer Model No-Load

For this transformer model it is known that the voltage, V is directly proportional to the number of turns by the change in magnetic flux over the change in time. As represented by the below formula.

$$V = N\frac{\partial \phi}{\partial t}$$

Where magnetic flux is represented by phi = Φ, number of turns =N, voltage=V and the time =t.

This model demonstrates that at steady state (ie when the transformer is operating under normal conditions after a long continuous period), that the voltage and magnetic flux are directly proportional. Subsequently the voltage and the current are also directly proportional. This can be shown as a representation of two waveforms, a voltage waveform and a magnetic flux waveform. Where Voltage=Sin(ωt) and Magnetic Flux=Cos(ωt) and is seen in figure 2.

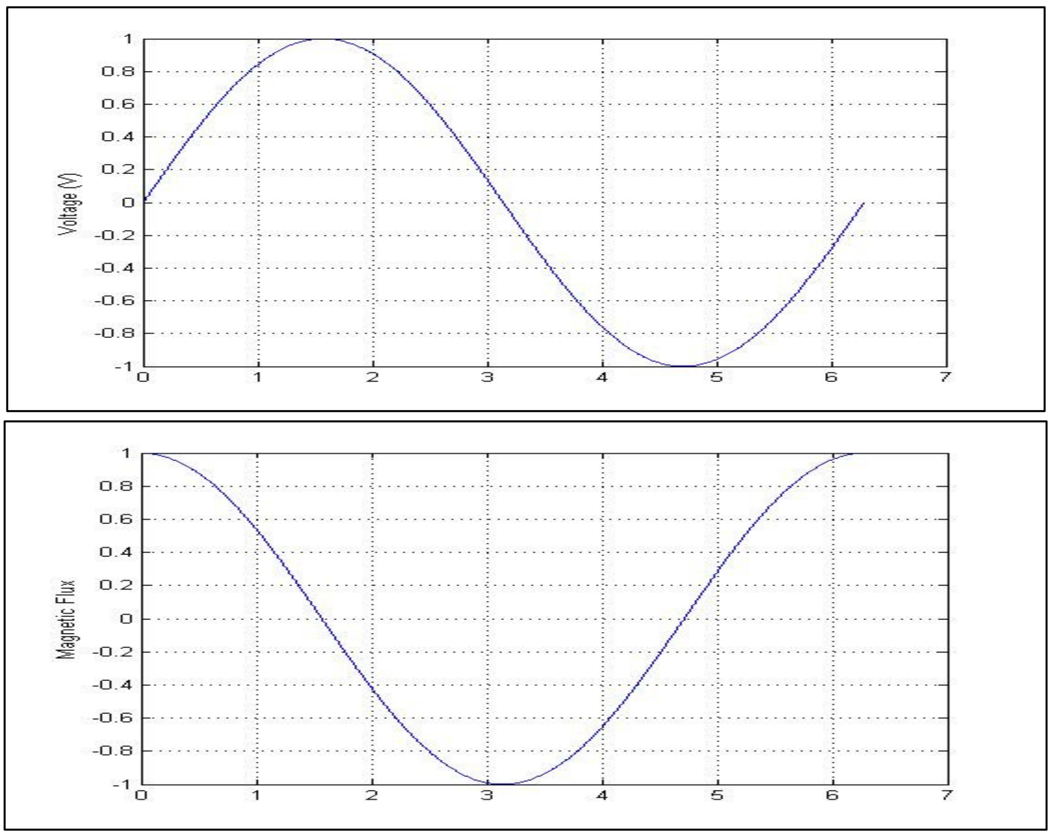

Figure 2 - Steady State Voltage and Magnetic Flux Waveforms

Using Ohm's law, current can be calculated by using the number of turns and the magnetic flux so that current becomes proportional to NΦ as per the below formula.

$$i \ \alpha \ N\Phi$$

This relationship, in a perfect situation would behave in a linear fashion. However the real relationship between current and magnetic flux is in a hysterisis loop arrangement. A real hysterisis loop of a test transformer at the University of Southern Queensland, performed by Dr Tony Ahfock, can be seen in figure 3. This diagram shows that the magnetic flux versus the current in a transformer does not follow a linear relationship but rather forms an envelope, hysterisis arrangement. It can also be seen that when the flux is very high, current can be tending towards infinitely high (shown by the flat line at the top of the hysterisis loop).

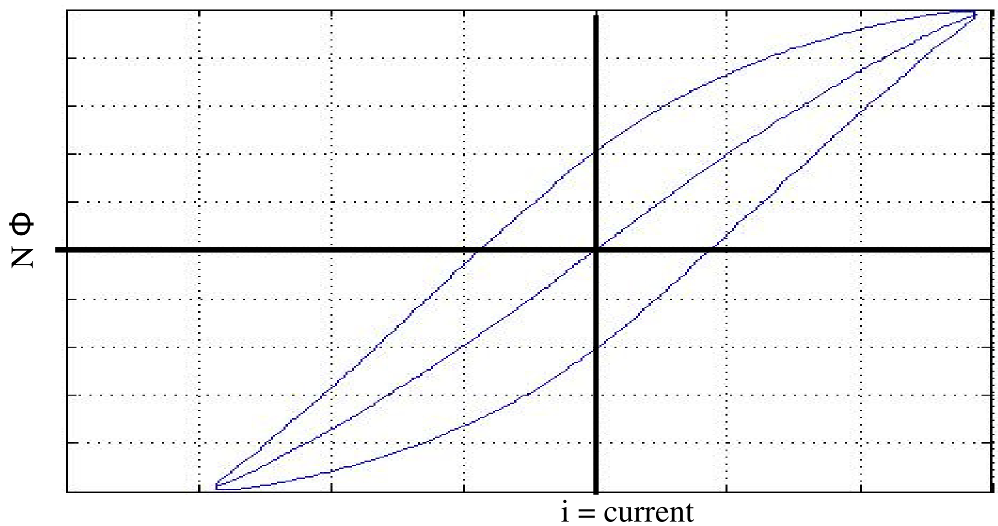

Figure 3 - Transformer Hysterisis Loop

Dr Tony Ahfock (USQ), along with students, has performed many tests on single and three phase transformers, analyzing the inrush current phenomenon. Figure 4 shows one such energisation. It can be seen in the diagram that the transformer has voltage applied to the primary side at approximately 0.052 seconds. It can also be seen that the time which the voltage is applied to the transformer is almost half way through one cycle of the AC voltage waveform. Additional information from the waveform is that the applied voltage is approximately 600Vpeak.

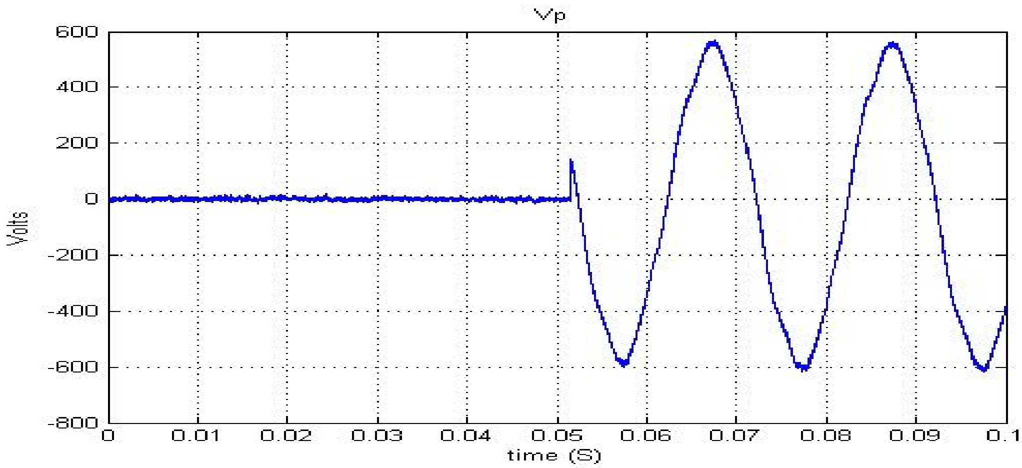

Figure 4 - Voltage Applied to Primary Side of Transformer

The corresponding current waveform is shown in Figure 5. In this diagram, two clear decaying peaks can be seen, with a third slightly obscured. The diagram also shows the current drawn reaching approximately 150A which is well above the rated current of this transformer. The first peak is delayed by approximately 0.01 seconds due to the lagging nature of the current. If this waveform was run till steady state, a smooth cosine shaped curve centered about the x-axis would be visible.

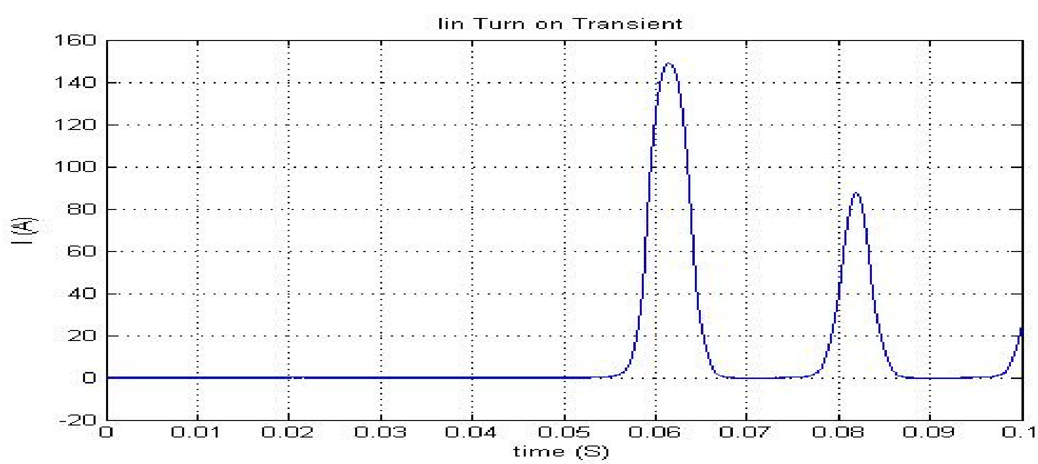

Figure 5 - Current Response to Input Voltage

2.2 Consequences of Inrush Current

Inrush current can have an adverse affect to the internal mechanical stresses exerted upon a transformer winding. The internal construction of a transformer is shown in Figure 6. It can be seen that within the transformer there exists many mechanical devices to support the transformer such as bolts, wedges and pre-pressed bandages. Stuerer and Frohlich (2002) found that, the design of these mechanical support structures is determined by the highest possible current peak which normally occurs under a short circuit condition. However the results of their study showed that inrush current peaks of approximately 70% of the rated short circuit current caused the same magnitude force as those at short circuit. Their study has also shown that although inrush currents normally are smaller than short circuit currents, the inrush current forces can be higher and for more extended periods of time.

Figure 6 - Internal design of a power transformer
(http://en.wikipedia.org/wiki/Transformer

This data causes alarm from a risk analysis and public safety perspective, as a transformer under inrush current has more force applied internally than originally designed for. This means that there is an increased risk of rupture to the windings destroying the asset or weakening the windings resulting in lower efficiency, or worst case, serious injury or death from an explosion of the windings.

2.3 Modern techniques for combating Inrush Current

Inrush current has been a factor of transformer design and switching for as long as the transformer has been in operation. Many techniques have been adopted and explored to understand the phenomenon and guard against the unhelpful results that inrush current has the potential to cause. The two most common techniques for minimising the effects of inrush current in power transformers are controlled switching and electronic relays. The third option, which is not as common in power transformers but is used commonly in switching power supplies, (Ametherm, http://www.ametherm.com/Inrush_Current/inrush_ current_faq.html) is the thermistor.

Controlled switching is the term used for the management of the magnitude of inrush current by energisation of the transformer, only when certain conditions are met. According to Basu and Asghar (2006), one method of controlled switching is delaying the close of the circuit breaker for each phase, which reduces the magnitude of inrush current drawn. This method of sequential switching is already in place in most modern high voltage circuit breakers as inbuilt inrush mitigation. Another form of controlled switching is to take advantage of the voltage and flux relationship. It is known from Section 2.1 that the voltage can be represented by a sine waveform and the flux by a cosine arrangement. It can be seen in Figure 2 that the maximum flux occurs at the positive going, zero crossing of the voltage waveform whereas the minimum flux occurs at the negative going, zero crossing of the voltage waveform for a single phase model. Using this relationship, Oliveira, Tavares and Apolonio (2006) have surmised that the inrush current drawn can be minimized when the above conditions are met. However they also note that the residual flux plays a key role in the determination of the inrush current, along with the three phase model also having dynamic flux (flux that is determined by the other phases). For standard power transformers, Brunke and Frohlich (2001) determine that due to the differences in statistical closing times and the effects of circuit breaker prestrikes, it is very difficult to energise a transformer at a specific instant. For these reasons and for reasons of practicality, the controlled switching, utilising the relationship of the flux to voltage is rarely incorporated into design for Power applications.

Thermistors are a passive circuit component used in sensitive switching power supplies. The thermistor operates as a current limiting device that provides resistance relative to a thermal threshold. As a thermistor heats, due to the increase in current (from the inrush current), it slowly decreases in resistance until the thermistor is at thermal maximum and the resistance is minor in terms of the overall system. Obviously this application of inrush current, surge limiting is not practical in a power application due to the relative size the component would have to be to provide any noticeable decrease in the magnitude of inrush current.

Finally, Electronic Relays are the most common modern inrush current monitoring device. These electronic relays do not change the magnitude of the inrush current drawn. However, they do minimise the effect that the large current draw has on the rest of the system. This is done by real time analysis of the current as it passes through the relay. If a surge current is detected by the relay, an analysis of the current for second harmonics is conducted. If the surge contains large second harmonics, it is neglected for a period of up to ten cycles. This process allows the relay to operate correctly and not cause a nuisance trip each time the transformer is energised. Relays and their application to inrush current are discussed further in Section 2.4.

2.4 Application of Electronic Differential Relays in Protection Systems

Differential protection relies on the principle of what comes into the transformer must also leave the transformer. This principle is applied to the current flow within a transformer. A simple diagram of how the differential protection system works is shown in Figure 7.

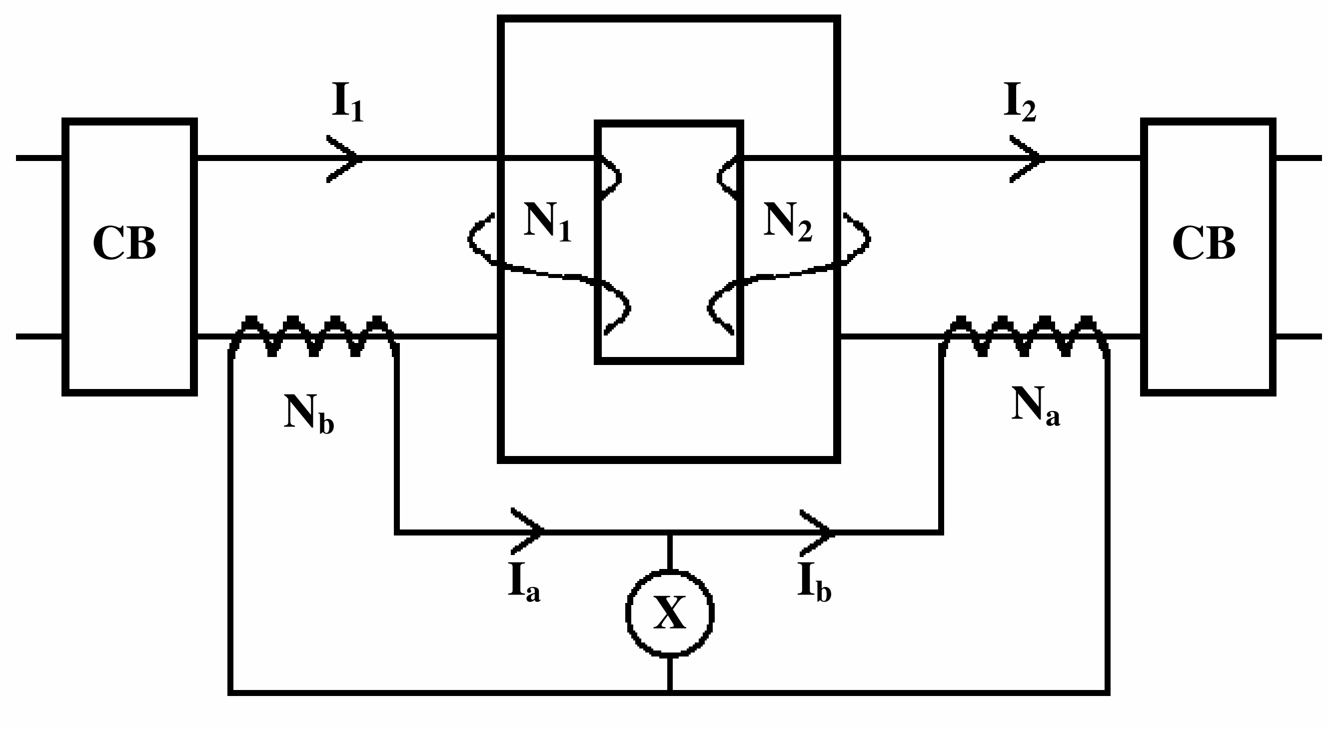

Figure 7 - Simplistic Differential Protection Schematic

Figure 7 shows that the differential protection system operates within the transformer circuit breakers. N_1 and N_2 represent the number of turns on the primary and secondary side of the transformer. I_1 and I_2 represent the current coming into and the current coming out of the transformer. N_a and N_b represent the windings on the current transformers (CT) that feed a "sample" or a "sniff" of the currents through the transformer by the currents I_a and I_b. The ratio of turns N_1:N_2 must be the same ratio, but not the same number of turns, as N_a:N_b. X represents a sensitive relay current sensor.

Put simply, when there is a fault inside the transformer (i.e. when what is going into the transformer is not coming out of the transformer) the CBs trip, isolating the transformer from the surrounding system and any source voltage and thus preventing any further damage. The system achieves this using the CTs at N_a and N_b and the relative currents I_a and I_b. When $I_1/I_2 \neq N_2/N_1$, $I_a \neq I_b$. Because the currents I_a do not equal I_b, current is forced to flow in the branch containing the sensitive current sensing relay, X (Kirchhoff's current law). The sensitive current relay is designed to detect any variance to its threshold and forces the circuit breakers to trip as mentioned.

At steady state or when the transformer is operating as normal, I_1/I_2 equals N_2/N_1 and subsequently I_a equals I_b. Because I_a equals I_b there is negligible current flow through the sensitive Current Sensing Relay and hence the circuit breakers will not trip.

The reason that differential protection is the cause of investigation is that inrush current, as described by Hunt, Schaefer and Bentert (2008), can cause a tripping of the differential protection systems as the relay believes it to be an internal fault. This type of tripping is regarded as a nuisance fault (for obvious reasons) and much despised amongst protection engineers in industry.

Protection Engineers have utilised many methods of avoiding nuisance tripping. One such method documented by Hunt, Schaefer and Bentert (2008) utilises and analyzes the current's second harmonic. They recommend that an analysis of the current to be computed by the differential relay and if the current has a high level of second harmonics to allow the current to pass for a further typical two to three cycles. This allows the transformer to keep operating during an inrush current "fault" but to still trip if another type of fault presents itself.

Hong and Qin (2000) contradict the usefulness of the second harmonic to determine inrush current faults. This is based on findings that with the increase in underground cables and overall higher capacities of distribution networks, there is a natural increase in the second harmonic. This makes other types of faults indistinguishable to inrush current. They are recommending further work be done in utilizing a wavelet based discrimination method thus avoiding the second harmonic issues arising.

The particular differential relay utilised commonly in transformer protection is the SEL-387A Current Differential and Overcurrent Relay. This relay protects two winding power transformers from differential faults, Overcurrent (OC) faults and also Restricted Earth Faults (REF). The relay is also able to track data such as breaker wear, battery monitoring, phase, ground, negative sequence, differential and harmonic metering and temperature metering. In addition to these functions, the relay will also provide event logs leading up to and including any tripping event.

CHAPTER 3: METHODOLOGY

This chapter outlines the project aims, objectives and the methodologies employed to accomplish them.

3.1 Project Aims and Objectives

The project aims are detailed in the Project Specification in Appendix A. The primary aim of this project is to investigate the inrush current phenomenon from a mathematical point of view and report on the findings. Those findings should include references to magnetic flux densities, harmonics and the magnitudes of the resultant currents (inrush current).

The secondary aim of this project is to develop a training package that is suitable to be used as a teaching package at USQ. This teaching package should include all relevant inrush current theory, differential relay data, practical experimentation information and also a set of review questions and answers. This teaching package should be appropriate to be included into a course designed for teaching transformer theory or protection theory.

The following core project objectives have been developed for fulfillment in this project and are addressed throughout the dissertation:

- Research inrush current test characteristics of power transformers
- Discuss with industry professionals and academics, the main features that are to be included in a transformer inrush current test facility.
- Design and build a transformer inrush current test rack that can be PLC controlled
- Program the PLC to conduct all inrush current test requirements including the use of protection relays

- Design and create the SCADA interface for the PLC and inrush current test environment
- Write full documentation on the design and operation the of the equipment suitable for use as a teaching course
- Develop and validate mathematical models to explain transformer inrush current
- Complete dissertation

3.2 Methodology of Objectives

Each of the Project aims has an associated methodology for completion.

3.2.1 Research Inrush Current test characteristics of Power Transformers

This objective is purely research based. To complete this objective, a thorough search of online, text based and journal sources needs to be conducted. Additionally the information and knowledge from USQ lecturers, specifically Dr Tony Ahfock, effectively is to be sourced and utilised in the completion of this objective.

3.2.2 Discuss with Industry Professionals and Academics, the main features that are to be included in a transformer Inrush Current test facility.

To complete this objective, discussion with Mr Bob Burgess and Dr Tony Ahfock will need to be conducted to determine what features the test rack that is currently in operation, already incorporates. Following that, investigation from the inrush current research will be analysed and utilised, along with recommendations from Dr Tony Ahfock to determine the appropriate features.

3.2.3 Design and build a transformer Inrush Current Test rack that can be PLC controlled

To complete this objective, the design features deemed appropriate from research and professionals is to be combined and drawn. The rack is to feature PLC control, Differential Relay Integration and remote access. Once the plans have been drawn, approval is to be sought for the construction of the test rack.

3.2.4 Program the PLC to conduct all Inrush Current test requirements including the use of protection relays

To complete this objective, PLC programming tutorials are to be conducted. The programming is to be designed to perform all inrush testing actions including the incorporation of the differential relay. Discussions with post-graduate students will also need to be conducted to ensure that this objective is not being hindered by similar works.

3.2.5 Design and create the SCADA interface for the PLC and Inrush Current test environment

To complete this objective, the PLC control is to be interfaced remotely through a SCADA panel. This SCADA programming will also require completion of a SCADA tutorial. Discussions with post-graduate students will also need to be conducted to ensure that this objective is not being hindered by similar works in the test rack environment.

3.2.6 Write full documentation on the design and operation of the equipment suitable for use as a teaching course

To achieve this objective, research on the appropriate writing style and format of a learning module will need to be undertaken. The teaching course material will need to incorporate the literature review that will be included in the dissertation along with all mathematical modeling completed. Students will be required to complete all relay setting calculations and perform tests on the transformer to visualize the inrush current phenomenon. Additionally the teaching module will provide review questions and answers.

3.2.7 Develop and validate mathematical models to explain transformer inrush current

To achieve this objective, inrush testing will need to occur. When reproducible tests are completed, the data is to be analysed using MATLAB. The analysis to be conducted includes performing an Fast Fourier Transform (FFT) on the inrush current data to provide evidence for inrush current harmonics, determination of peak inrush current and also an approximation of the inrush current decay time.

3.2.8 Complete dissertation

To achieve this objective, a plan will need to be created as to what the dissertation is to accomplish. The formal writing will need to begin approximately two months before the due date of the dissertation and will take approximately 60 hours to complete.

CHAPTER 4: FUNCTIONALITIES OF THE DIFFERENTIAL RELAY

This chapter outlines the functionalities and purposes of a differential relay in modern transformer protection. It does this by describing the normal operations of the SEL-387A Current Differential Relay and also by describing each of the settings and what they control. This chapter also describes how to design the settings related to inrush current for a SEL-387A Current Differential Relay.

4.1 Purpose and Functions of a Current Differential Relay

As described in Chapter 2, the differential relay is a device that prevents damage to the asset (transformer) that its sensors are either side of. This is achieved through making an assumption that the current traveling into a transformer, after slight losses, must proportionally exit the asset.

The differential relay that is the focus of this dissertation is the Schweitzer Engineering Laboratories, SEL-387A Current Differential and Overcurrent Protection Relay. This relay can protect assets such as transformers, buses, generators, reactors from current differentials, overcurrent and also temperature threshold protection. Additionally the relay has the capacity to be utilised as a restricted earth fault protection device. A front and rear view of this relay is shown in figure 8.

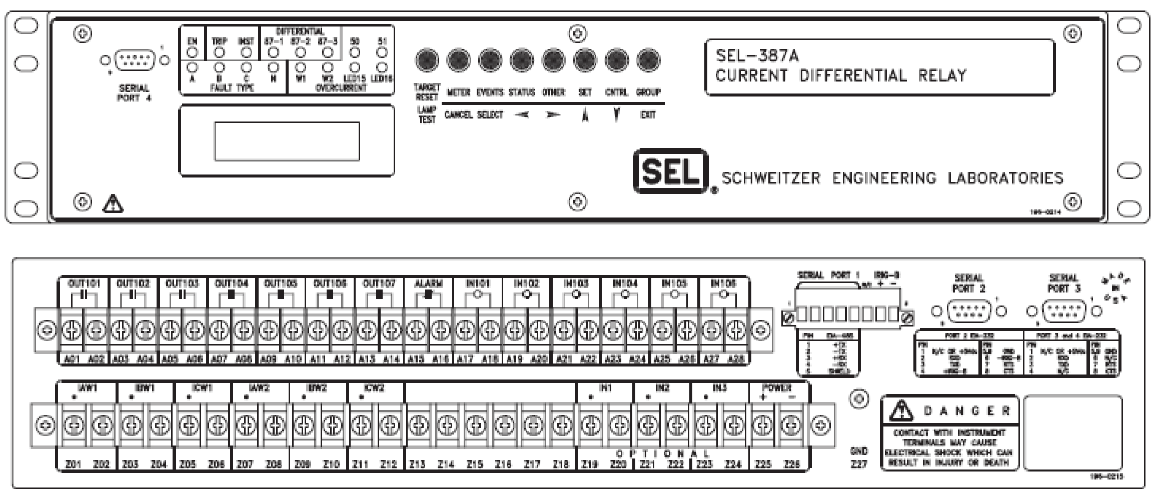

Figure 8 - Front and Rear view of the SEL-387A Relay

The SEL-387A relay is used in conjunction with asset circuit breakers. To perform a trip, the relay senses a fault or past threshold conditions and communicates for the circuit breakers to trip either side of the asset. This tripping isolates the asset from any further input current and outgoing current draw. According the Schweitzer Engineering Laboratories data sheets, the maximum time of pick up on any fault is 2.86 cycles or at 50Hz, approximately 5.72 milliseconds. Isolations of this nature are extremely effective at reducing the damage due to severe faults, especially on power transformers. As well as providing the circuit break order, the relay records the system data such as current and phase angles leading up to and including the tripping of the circuit breaker. This makes the SEL-387A also useful in fault analysis and determining the source (based on the magnitude, phase and angle of the current) that caused the fault.

A differential relay of the nature described above is often referred to as a SMART relay due to their micro-processor control, but also because of the supplementary features they can offer a user. Some of these features include instantaneous phase and current measurements, peak demand data, circuit breaker information such as breaker wear and also battery monitoring (in some applications). The secondary reasoning for being termed “SMART” relays is that they can be interfaced using SCADA. This feature allows user to be remote of the relay’s location and still access the data and tripping notifications. Additionally the relay can be reset remotely allowing full operation of the relay and asset without a physical inspection NB this practice would not be employed every time due to Occupational Health and Safety policies regarding inspection of tripped assets to ensure no auxiliary issues are present or are the cause.

The feature of the SEL-387A important to this dissertation is the harmonic detection features of the relay. The 2^{nd}, 4^{th} and 5^{th} harmonic detection allows for the detection of currents that represent the high surge currents caused by inrush or overexcitation conditions. Due to the nature of the inrush being a very large current draw from “inside” the transformer, normally this would be regarded as a fault according to the differential protection principle. Because it is a fault, a subsequent operation of the circuit breaker would occur. This trip of the circuit breaker is what is referred to as a “nuisance” trip because it has not tripped on an abnormal fault. To prevent nuisance tripping, inrush conditions are detected by the setting of the even harmonics to a threshold of between 5% and 100%. If a surge is detected by the relay, but the ratio of the second and/or fourth harmonics to the fundamental harmonic is greater than the set threshold, the relay will not issue a trip breaker command for as many cycles as the surge still contains a ratio of above threshold harmonics.

4.2 SEL-387A Protection Relay setting guide

The SEL-387A protection relay has a multitude of settings that are inputted to ensure that the relay is correctly configured to operate on the specific asset that it is connected to. There are over 600 settable options on the SEL-387A relay to ensure correct operation. These settings range from naming the relay, setting the conditions of the LED indicators being lit to determining the number of turns on the current transformer (CT). Accurate and careful programming of the settings is paramount in efficient and correct operation of the relay.

Table 1 is a summary of operation for each of the relay settings. All of the associated logic diagrams for all of these settings can be found in the SEL-387A Differential Relay Instruction Manual.

Table 1: Summary of operation of each SEL-387A relay setting

Setting Description	**Setting Name**	**Comments**
Relay Identifier (39 Characters Maximum)	RID	Data for the identification of the relay
Terminal Identifier (59 Characters Maximum)	TID	
Enable Differential Element (Y, N)	E87	These settings allow for parent control of the specific settings for each of the relay features.
Enable Winding 1 O/C Elements and Dmd Thresholds (Y, N)	EOC1	
Enable Winding 2 O/C Elements and Dmd Thresholds (Y, N)	EOC2	
Enable Winding Neutral Elements (Y, N)	EOCN	
Enable RTDA Element (Y, N)	E49A	
Enable RTDB Element (Y, N)	E49B	
Enable SELogic® Control Equations Set 1 (Y, N)	ESLS1	
Enable SELogic Control Equations Set 2 (Y, N)	ESLS2	
Enable SELogic Control Equations Set 3 (Y, N)	ESLS3	
General Data		
Winding 1 CT Connection (D, Y)	W1CT	Sets the winding configuration as delta or star. Must be set to star to take advantage of the metering capabilities of the SEL387A
Winding 2 CT Connection (D, Y)	W2CT	
Winding 1 CT Ratio (1–50000)	CTR1	Sets the ratio of turns for the 1st and 2nd winding, Current transformers
Winding 2 CT Ratio (1–50000)	CTR2	
Neutral 1 CT Ratio (1–50000)	CTRN1	Sets the turns ratio for the neutral CTs for up to three neutrals
Neutral 2 CT Ratio (1–50000)	CTRN2	

Neutral 3 CT Ratio (1–50000)	CTRN3	
Maximum Power Xfmr Capacity (OFF, 0.2–5000.0 MVA)	MVA	Sets the maximum power the transformer would be subject to
Define Internal CT Connection Compensation (Y, N)	ICOM	Allows for internal compensation for the CT
Winding 1 CT Conn. Compensation (0, 1, …, 12)	W1CTC	Relay vector shift and zero sequence compensation shifts for winding CT compensation
Winding 2 CT Conn. Compensation (0, 1, …, 12)	W2CTC	
Winding 1 Line-to-Line Voltage (1.00–1000.00 kV)	VWDG1	Set to the nominal voltage of the power transformer winding.
Winding 2 Line-to-Line Voltage (1.00–1000.00 kV)	VWDG2	
Differential Elements		
Note: TAP1 and TAP2 are auto-set by relay if MVA setting is not OFF.		
Winding 1 Current Tap (0.10–31.00 A secondary) (1 A)	TAP1	These settings are auto-set via the Maximum Power Xfmr Capacity setting
Winding 2 Current Tap (0.10–31.00 A secondary) (1 A)	TAP2	
Restrained Element Operating Current PU (0.10–1.00 TAP)	O87P	These settings relate to the overall differential protection characteristics. The particular settings relate to the threshold of operation such that O87P is the minimum "operate" level for operation, SLP1 is the initial slope of the relay curve that begins at the origin and intersects O87P at IRT=O87P*100/SLP1. Also IRS1 is the limit of SLP1for operation (beginning of SLP2) and SLP2 is the second slope and must be equal to or greater that SLP1 for normal curve plotting.
Restraint Slope 1 Percentage (5–100%)	SLP1	
Restraint Slope 2 Percentage (OFF, 25–200%)	SLP2	
Restraint Current Slope 1 Limit (1.0–20.0 TAP)	IRS1	
Unrestrained Element Current PU (1–20 TAP)	U87P	This setting allows for quick reaction to very high currents that are obvious faults. This setting can be tripped by inrush, therefore needs to be set higher than expected inrush magnitude.
Second-Harmonic Blocking Percentage (OFF, 5–100%)	PCT2	These settings directly relate to the discernment of inrush current due to inrush current having high values of 2nd and 4th harmonics. These settings are ratios of the second or fourth harmonic magnitude divided by the fundamental magnitude.
Fourth-Harmonic Blocking Percentage (OFF, 5–100%)	PCT4	
Fifth-Harmonic Blocking Percentage (OFF, 5–100%)	PCT5	These settings relate to over-excitation. Over-excitation produces odd harmonics and PCT5 allows for the setting of the core flux density ratio. TH5P and TH5D allow for an alarm and pickup delay for these types of conditions.
Fifth-Harmonic Alarm Threshold (OFF, 0.02–3.2 TAP)	TH5P	
Fifth-Harmonic Alarm TDPU (0.000–8000.000 cyc)	TH5D	
DC Ratio Blocking (Y, N)	DCRB	This setting allows for the control of a DC offset suitable for the detection of some inrush current conditions that do not exhibit even harmonics.

Harmonic Restraint (Y, N)	HRSTR	This allows for the relay to detect the second and fourth harmonics independently and on trip if the combination of both exceeds the sum threshold but not for 2nd or 4th harmonics independently.
Independent Harmonic Blocking (Y, N)	IHBL	Activates harmonic blocking on phases independently that they are detected on, not for all three phases.
Restricted Earth Fault		
Enable 32I (SELogic control equation)	E32I1	Enables REF1
Operating Quantity from Wdg. 1, Wdg. 2 (1, 2, 12)	32IOP1	Indicates which winding is being monitored
Positive-Sequence Current Restraint Factor, I0/I1 (0.02–0.50)	a01	Settings for the detection of the REF fault (1)
Residual Current Sensitivity Threshold (0.05–3 A secondary) (1 A)	50GP1	
Enable 32I (SELogic control equation)	E32I2	Enables REF2
Operating Quantity from Wdg. 1, Wdg. 2 (1, 2, 12)	32IOP2	Indicates which winding is being monitored
Positive-Sequence Current Restraint Factor, I0/I1 (0.02–0.50)	a02	Settings for the detection of the REF fault (2)
Residual Current Sensitivity Threshold (0.05–3 A secondary) (1 A)	50GP2	
Winding 1 O/C Elements		
Winding 1 Phase O/C Elements		
Phase Def.-Time O/C Level 1 PU (OFF, 0.05–20 A secondary) (1 A)	50P11P	Relates to the definite time element of the O/C protection and is dictated by the SELogic 50Pn1TC equation as to whether currents of higher magnitude than this setting should trip
Phase Level 1 O/C Delay (0.00–16000.00 cycles)	50P11D	Relates to the operation of 50Pn1P in only allowing a trip if the magnitude of current that is above threshold is maintained for the entirety of the delay setting
50P11 Torque Control (SELogic control equation)	50P11TC	The control equation for 50Pn1P
Phase Inst. O/C Level 2 PU (OFF, 0.05–20 A secondary) (1 A)	50P12P	This setting relates to Instantaneous O/C element and is dictated by the torque-controlled SELogic 50PnTC equation as to whether the exceeded threshold constitutes a trip
50P12 Torque Control (SELogic control equation)	50P12TC	The control equation for 50Pn2P
Phase Inst. O/C Level 3 PU (OFF, 0.05–20 A secondary) (1 A)	50P13P	These settings are non-torque controlled settings that are a simple monitoring of the phases to determined whether the magnitude has been exceeded
Phase Inst. O/C Level 4 PU (OFF, 0.05–20 A secondary) (1 A)	50P14P	
Phase Inv.-Time O/C PU (OFF, 0.10–3.20 A secondary) (1 A)	51P1P	These settings determine the inverse time O/C element torque controlled pickup settings. The 51PnP relates to the threshold dictated by the SELogic
Phase Inv.-Time O/C Curve (U1–U5, C1–C5)	51P1C	
Phase Inv.-Time O/C Time-Dial (US 0.5–15.0, IEC	51P1TD	

0.05–1.00)		control equation 51PnTC while the 51PnC, 51PnTD and 51PnRS relates the curve and timing characteristics of the setting logic.
Phase Inv.-Time O/C EM Reset (Y, N)	51P1RS	
51P1 Torque Control (SELogic control equation)	51P1TC	The control equation for pickup of 51PnP
Winding 1 Negative-Sequence O/C Elements		
Note: All negative-sequence element pickup settings are in terms of $3I_2$.		
Neg.-Seq. Def.-Time O/C Level 1 PU (OFF, 0.05–20 A secondary) (1 A)	50Q11P	The same principle of operation as 50Pn1P
Neg.-Seq. Level 1 O/C Delay (0.50–16000.00 cycles)	50Q11D	The same principle of operation as 50Pn1D
50Q11 Torque Control (SELogic control equation)	50Q11TC	The control equation for 50Qn1P
Neg.-Seq. Inst. O/C Level 2 PU (OFF, 0.05–20 A secondary) (1 A)	50Q12P	The same principle of operation as 50Pn2P
50Q12 Torque Control (SELogic control equation)	50Q12TC	The control equation for 50Qn2P
Neg.-Seq. Inv.-Time O/C PU (OFF, 0.10–3.20 A secondary) (1 A)	51Q1P	The same principle of operation as 51PnP, 51PnC, 51PnTD and 51PnRS
Neg.-Seq. Inv.-Time O/C Curve (U1–U5, C1–C5)	51Q1C	
Neg.-Seq. Inv.-Time O/C Time-Dial (US 0.5–15, IEC 0.05–1.00)	51Q1TD	
Neg.-Seq. Inv.-Time O/C EM Reset (Y, N)	51Q1RS	
51Q1 Torque Control (SELogic control equation)	51Q1TC	The control equation for 51QnP
Winding 1 Residual O/C Elements		
Residual Def.-Time O/C Level 1 PU (OFF, 0.05–20 A secondary) (1 A)	50N11P	The same principle of operation as 50Pn1P
Residual Level 1 O/C Delay (0.00–16000.00 cycles)	50N11D	The same principle of operation as 50Pn1D
50N11 Torque Control (SELogic control equation)	50N11TC	The control equation for 50Nn1P
Residual Inst. O/C Level 2 PU (OFF, 0.05–20 A secondary) (1 A)	50N12P	The same principle of operation as 50Pn2P
50N12 Torque Control (SELogic control equation)	50N12TC	The control equation for 50Nn2P
Residual Inv.-Time O/C PU (OFF, 0.10–3.20 A secondary) (1 A)	51N1P	The same principle of operation as 51PnP, 51PnC, 51PnTD and 51PnRS
Residual Inv.-Time O/C Curve (U1–U5, C1–C5)	51N1C	
Residual Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00)	51N1TD	
Residual Inv.-Time O/C EM Reset (Y, N)	51N1RS	
51N1 Torque Control (SELogic control equation)	51N1TC	The control equation for 51NnP
Winding 1 Demand Metering		
Demand Ammeter Time Constant (OFF, 5–255 min)	DATC1	These settings dictate the threshold current demand. If these values are exceeded the indications can be used as an alert through the front panel LEDs or through SCADA
Phase Demand Ammeter Threshold (0.10–3.20 A secondary) (1 A)	PDEM1P	
Neg.-Seq. Demand Ammeter Threshold (0.10–3.20 A secondary) (1 A)	QDEM1P	
Residual Demand Ammeter Threshold (0.10–3.20 A secondary) (1 A)	NDEM1P	
Winding 2 O/C Elements		
Winding 2 Phase O/C Elements		

Phase Def.-Time O/C Level 1 PU (OFF, 0.05–20 A secondary) (1 A)	50P21P	Relates to the definite time element of the O/C protection and is dictated by the SELogic 50Pn1TC equation as to whether currents of higher magnitude than this setting should trip
Phase Level 1 O/C Delay (0.00–16000.00 cycles)	50P21D	Relates to the operation of 50Pn1P in only allowing a trip if the magnitude of current that is above threshold is maintained for the entirety of the delay setting
50P21 Torque Control (SELogic control equation)	50P21TC	The control equation for 50Pn1P
Phase Inst. O/C Level 2 PU (OFF, 0.05–20 A secondary) (1 A)	50P22P	This setting relates to Instantaneous O/C element and is dictated by the torque-controlled SELogic 50PnTC equation as to whether the exceeded threshold constitutes a trip
50P22 Torque Control (SELogic control equation)	50P22TC	The control equation for 50Pn2P
Phase Inst. O/C Level 3 PU (OFF, 0.05–20 A secondary) (1 A)	50P23P	These settings are non-torque controlled settings that are a simple monitoring of the phases to determined whether the magnitude has been exceeded
Phase Inst. O/C Level 4 PU (OFF, 0.05–20 A secondary) (1 A)	50P24P	
Phase Inv.-Time O/C PU (OFF, 0.10–3.20 A secondary) (1 A)	51P2P	These settings determine the inverse time O/C element torque controlled pickup settings. The 51PnP relates to the threshold dictated by the SELogic control equation 51PnTC while the 51PnC, 51PnTD and 51PnRS relates the curve and timing characteristics of the setting logic.
Phase Inv.-Time O/C Curve (U1–U5, C1–C5)	51P2C	
Phase Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00)	51P2TD	
Phase Inv.-Time O/C EM Reset (Y, N)	51P2RS	
51P2 Torque Control (SELogic control equation)	51P2TC	The control equation for pickup of 51PnP
Winding 2 Negative-Sequence O/C Elements		
Note: All negative-sequence element pickup settings are in terms of $3I_2$.		
Neg.-Seq. Def.-Time O/C Level 1 PU(OFF, 0.05–20 A secondary) (1 A)	50Q21P	The same principle of operation as 50Pn1P
Neg.-Seq. Level 1 O/C Delay (0.50–16000.00 cycles)	50Q21D	The same principle of operation as 50Pn1D
50Q21 Torque Control (SELogic control equation)	50Q21TC	The control equation for 50Qn1P
Neg.-Seq. Inst. O/C Level 2 PU (OFF, 0.05–20 A secondary) (1 A)	50Q22P	The same principle of operation as 50Pn2P
50Q22 Torque Control (SELogic control equation)	50Q22TC	The control equation for 50Qn2P
Neg.-Seq. Inv.-Time O/C PU (OFF, 0.10–3.20 A secondary) (1 A)	51Q2P	The same principle of operation as 51PnP, 51PnC, 51PnTD and 51PnRS
Neg.-Seq. Inv.-Time O/C Curve (U1–U5, C1–C5)	51Q2C	
Neg.-Seq. Inv.-Time O/C Time-Dial (US 0.5–15, IEC 0.05–1.00)	51Q2TD	
Neg.-Seq. Inv.-Time O/C EM Reset (Y, N)	51Q2RS	
51Q2 Torque Control (SELogic control equation)	51Q2TC	The control equation for 51QnP
Winding 2 Residual O/C Elements		
Residual Def.-Time O/C Level 1 PU (OFF, 0.05–20 A secondary) (1 A)	50N21P	The same principle of operation as 50Pn1P

Residual Level 1 O/C Delay (0.00–16000.00 cycles)	50N21D	The same principle of operation as 50Pn1D
50N21 Torque Control (SELogic control equation)	50N21TC	The control equation for 50Nn1P
Residual Inst. O/C Level 2 PU (OFF, 0.05–20 A secondary) (1 A)	50N22P	The same principle of operation as 50Pn2P
50N22 Torque Control (SELogic control equation)	50N22TC	The control equation for 50Nn2P
Residual Inv.-Time O/C PU (OFF, 0.10–3.20 A secondary) (1 A)	51N2P	The same principle of operation as 51PnP, 51PnC, 51PnTD and 51PnRS
Residual Inv.-Time O/C Curve (U1–U5, C1–C5)	51N2C	
Residual Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00)	51N2TD	
Residual Inv.-Time O/C EM Reset (Y, N)	51N2RS	
51N2 Torque Control (SELogic control equation)	51N2TC	The control equation for 51NnP
Winding 2 Demand Metering		
Demand Ammeter Time Constant (OFF, 5–255 min)	DATC2	These settings dictate the threshold current demand. If these values are exceeded the indications can be used as an alert through the front panel LEDs or through SCADA
Phase Demand Ammeter Threshold (0.10–3.20 A secondary) (1 A)	PDEM2P	
Neg.-Seq. Demand Ammeter Threshold (0.10–3.20 A secondary) (1 A)	QDEM2P	
Residual Demand Ammeter Threshold (0.10–3.20 A secondary) (1 A)	NDEM2P	
Neutral Elements		
Neutral 1 Elements		
Neutral Def.-Time O/C Level 1 PU (OFF, 0.05–20 A secondary) (1 A)	50NN11P	Relates to the definite time element of the O/C protection and is dictated by the SELogic 50NNn1TC equation as to whether currents of higher magnitude than this setting should trip
Neutral Level 1 O/C Delay (0.00–16000.00 cycles)	50NN11D	Relates to the operation of 50NNn1P in only allowing a trip if the magnitude of current that is above threshold is maintained for the entirety of the delay setting
50NN11 Torque Control (SELogic control equation)	50NN11TC	The control equation for 50NNn1P
Neutral Inst. O/C Level 2 PU(OFF, 0.05–20 A secondary) (1 A)	50NN12P	This setting relates to Instantaneous O/C element and is dictated by the torque-controlled SELogic 50NNnTC equation as to whether the exceeded threshold constitutes a trip
50NN12 Torque Control (SELogic control equation)	50NN12T	The control equation of 50NNn2P
Neutral Inst. O/C Level 3 PU(OFF, 0.05–20 A secondary) (1 A)	50NN13P	These settings are non-torque controlled settings that are a simple monitoring of the phases to determined whether the magnitude has been exceeded
Neutral Inst. O/C Level 4 PU (OFF, 0.05–20 A secondary) (1 A)	50NN14P	
Neutral Inv.-Time O/C PU (OFF, 0.10–3.20 A secondary) (1 A)	51NN1P	These settings determine the inverse time O/C element torque controlled pickup settings. The 51NNnP relates to the threshold dictated by the SELogic control equation
Neutral Inv.-Time O/C Curve (U1–U5, C1–C5)	51NN1C	
Neutral Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00)	51NN1TD	

Neutral Inv.-Time O/C EM Reset (Y, N)	51NN1RS	51NNPnTC while the 51NNnC, 51NNnTD and 51NNnRS relates the curve and timing characteristics of the setting logic.
51NN1 Torque Control (SELogic control equation)	51NN1TC	The control equation for pickup of 51NNnP
Neutral 2 Elements		
Neutral Def.-Time O/C Level 1 PU (OFF, 0.05–20 A secondary) (1 A)	50NN21P	Relates to the definite time element of the O/C protection and is dictated by the SELogic 50NNn1TC equation as to whether currents of higher magnitude than this setting should trip
Neutral Level 1 O/C Delay (0.00–16000.00 cycles)	50NN21D	Relates to the operation of 50NNn1P in only allowing a trip if the magnitude of current that is above threshold is maintained for the entirety of the delay setting
50NN21 Torque Control (SELogic control equation)	50NN21TC	The control equation for 50NNn1P
Neutral Inst. O/C Level 2 PU(OFF, 0.05–20 A secondary) (1 A)	50NN22P	This setting relates to Instantaneous O/C element and is dictated by the torque-controlled SELogic 50NNnTC equation as to whether the exceeded threshold constitutes a trip
50NN22 Torque Control (SELogic control equation)	50NN22T	The control equation for 50NNn2P
Neutral Inst. O/C Level 3 PU(OFF, 0.05–20 A secondary) (1 A)	50NN23P	These settings are non-torque controlled settings that are a simple monitoring of the phases to determined whether the magnitude has been exceeded
Neutral Inst. O/C Level 4 PU (OFF, 0.05–20 A secondary) (1 A)	50NN24P	
Neutral Inv.-Time O/C PU (OFF, 0.10–3.20 A secondary) (1 A)	51NN2P	These settings determine the inverse time O/C element torque controlled pickup settings. The 51NNnP relates to the threshold dictated by the SELogic control equation 51NNPnTC while the 51NNnC, 51NNnTD and 51NNnRS relates the curve and timing characteristics of the setting logic.
Neutral Inv.-Time O/C Curve (U1–U5, C1–C5)	51NN2C	
Neutral Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00)	51NN2TD	
Neutral Inv.-Time O/C EM Reset (Y, N)	51NN2RS	
51NN2 Torque Control (SELogic control equation)	51NN2TC	The control equation for pickup of 51NNnP
Neutral 3 Elements		
Neutral Def.-Time O/C Level 1 PU (OFF, 0.05–20 A secondary) (1 A)	50NN31P	Relates to the definite time element of the O/C protection and is dictated by the SELogic 50NNn1TC equation as to whether currents of higher magnitude than this setting should trip
Neutral Level 1 O/C Delay (0.00–16000.00 cycles)	50NN31D	Relates to the operation of 50NNn1P in only allowing a trip if the magnitude of current that is above threshold is maintained for the entirety of the delay setting

50NN31 Torque Control (SELogic control equation)	50NN31TC	The control equation for 50NNn1P
Neutral Inst. O/C Level 2 PU (OFF, 0.05–20 A secondary) (1 A)	50NN32P	This setting relates to Instantaneous O/C element and is dictated by the torque-controlled SELogic 50NNnTC equation as to whether the exceeded threshold constitutes a trip
50NN32 Torque Control (SELogic control equation)	50NN32TC	The control equation for 50NNn2P
Neutral Inst. O/C Level 3 PU (OFF, 0.05–20 A secondary) (1 A)	50NN33P	These settings are non-torque controlled settings that are a simple monitoring of the phases to determined whether the magnitude has been exceeded
Neutral Inst. O/C Level 4 PU (OFF, 0.05–20 A secondary) (1 A)	50NN34P	
Neutral Inv.-Time O/C PU (OFF, 0.10–3.20 A secondary) (1 A)	51NN3P	These settings determine the inverse time O/C element torque controlled pickup settings. The 51NNnP relates to the threshold dictated by the SELogic control equation 51NNPnTC while the 51NNnC, 51NNnTD and 51NNnRS relates the curve and timing characteristics of the setting logic.
Neutral Inv.-Time O/C Curve (U1–U5, C1–C5)	51NN3C	
Neutral Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00)	51NN3TD	
Neutral Inv.-Time O/C EM Reset (Y, N)	51NN3RS	
51NN3 Torque Control (SELogic control equation)	51NN3TC	The control equation for pickup of 51NNnP
RTD A Elements		
RTD 1A Alarm Temperature (OFF, 32–482°F)	49A01A	These settings allow for the control of the temperature value for alarm and trip operations in association with the SEL-2600s. Turned off and on by the E49A setting.
RTD 1A Trip Temperature (OFF, 32–482°F)	49T01A	
RTD 2A Alarm Temperature (OFF, 32–482°F)	49A02A	
RTD 2A Trip Temperature (OFF, 32–482°F)	49T02A	
RTD 3A Alarm Temperature (OFF, 32–482°F)	49A03A	
RTD 3A Trip Temperature (OFF, 32–482°F)	49T03A	
RTD 4A Alarm Temperature (OFF, 32–482°F)	49A04A	
RTD 4A Trip Temperature (OFF, 32–482°F)	49T04A	
RTD 5A Alarm Temperature (OFF, 32–482°F)	49A05A	
RTD 5A Trip Temperature (OFF, 32–482°F)	49T05A	
RTD 6A Alarm Temperature (OFF, 32–482°F)	49A06A	
RTD 6A Trip Temperature (OFF, 32–482°F)	49T06A	
RTD 7A Alarm Temperature (OFF, 32–482°F)	49A07A	
RTD 7A Trip Temperature (OFF, 32–482°F)	49T07A	
RTD 8A Alarm Temperature (OFF, 32–482°F)	49A08A	
RTD 8A Trip Temperature (OFF, 32–482°F)	49T08A	
RTD 9A Alarm Temperature (OFF, 32–482°F)	49A09A	
RTD 9A Trip Temperature (OFF, 32–482°F)	49T09A	
RTD 10A Alarm Temperature (OFF, 32–482°F)	49A10A	
RTD 10A Trip Temperature (OFF, 32–482°F)	49T10A	
RTD 11A Alarm Temperature (OFF, 32–482°F)	49A11A	
RTD 11A Trip Temperature (OFF, 32–482°F)	49T11A	
RTD 12A Alarm Temperature (OFF, 32–482°F)	49A12A	
RTD 12A Trip Temperature (OFF, 32–482°F)	49T12A	

RTD B Elements		
RTD 1B Alarm Temperature (OFF, 32–482°F)	49A01B	These settings allow for the control of the temperature value for alarm and trip operations in association with the SEL-2600s. Turned on and off by the E49B setting.
RTD 1B Trip Temperature (OFF, 32–482°F)	49T01B	
RTD 2B Alarm Temperature (OFF, 32–482°F)	49A02B	
RTD 2B Trip Temperature (OFF, 32–482°F)	49T02B	
RTD 3B Alarm Temperature (OFF, 32–482°F)	49A03B	
RTD 3B Trip Temperature (OFF, 32–482°F)	49T03B	
RTD 4B Alarm Temperature (OFF, 32–482°F)	49A04B	
RTD 4B Trip Temperature (OFF, 32–482°F)	49T04B	
RTD 5B Alarm Temperature (OFF, 32–482°F)	49A05B	
RTD 5B Trip Temperature (OFF, 32–482°F)	49T05B	
RTD 6B Alarm Temperature (OFF, 32–482°F)	49A06B	
RTD 6B Trip Temperature (OFF, 32–482°F)	49T06B	
RTD 7B Alarm Temperature (OFF, 32–482°F)	49A07B	
RTD 7B Trip Temperature (OFF, 32–482°F)	49T07B	
RTD 8B Alarm Temperature (OFF, 32–482°F)	49A08B	
RTD 8B Trip Temperature (OFF, 32–482°F)	49T08B	
RTD 9B Alarm Temperature (OFF, 32–482°F)	49A09B	
RTD 9B Trip Temperature (OFF, 32–482°F)	49T09B	
RTD 10B Alarm Temperature (OFF, 32–482°F)	49A10B	
RTD 10B Trip Temperature (OFF, 32–482°F)	49T10B	
RTD 11B Alarm Temperature (OFF, 32–482°F)	49A11B	
RTD 11B Trip Temperature (OFF, 32–482°F)	49T11B	
RTD 12B Alarm Temperature (OFF, 32–482°F)	49A12B	
RTD 12B Trip Temperature (OFF, 32–482°F)	49T12B	
Miscellaneous Timers		
Minimum Trip Duration Time Delay (4.000–8000.000 cycles)	TDURD	Controls the minimum time that the relay will operate a trip for (in cycles)
Close Failure Logic Time Delay (OFF, 0.000–8000.000 cycles)	CFD	Setting to only allow the breaker close logic to be maintained for a dictated number of cycles
SELogic Control Equations Set 1		
Set 1 Variable 1 (SELogic control equation)	S1V1	These settings allow for the definitions of the SELogic control equations including their associated timer pickup and dropout times
S1V1 Timer Pickup (OFF, 0.000–999999.000 cycles)	S1V1PU	
S1V1 Timer Dropout (OFF, 0.000–999999.000 cycles)	S1V1DO	
Set 1 Variable 2 (SELogic control equation)	S1V2	
S1V2 Timer Pickup (OFF, 0.000–999999.000 cycles)	S1V2PU	
S1V2 Timer Dropout (OFF, 0.000–999999.000 cycles)	S1V2DO	
Set 1 Variable 3 (SELogic control equation)	S1V3	
S1V3 Timer Pickup (OFF, 0.000–999999.000 cycles)	S1V3PU	
S1V3 Timer Dropout (OFF, 0.000–999999.000 cycles)	S1V3DO	
Set 1 Variable 4 (SELogic control equation)	S1V4	

S1V4 Timer Pickup (OFF, 0.000–999999.000 cycles)	S1V4PU	
S1V4 Timer Dropout (OFF, 0.000–999999.000 cycles)	S1V4DO	
Set 1 Latch Bit 1 SET Input (SELogic control equation)	S1SLT1	These settings dictate the latch set and reset values for the SELogic equations defined above.
Set 1 Latch Bit 1 RESET Input (SELogic control equation)	S1RLT1	
Set 1 Latch Bit 2 SET Input (SELogic control equation)	S1SLT2	
Set 1 Latch Bit 2 RESET Input (SELogic control equation)	S1RLT2	
Set 1 Latch Bit 3 SET Input (SELogic control equation)	S1SLT3	
Set 1 Latch Bit 3 RESET Input (SELogic control equation)	S1RLT3	
Set 1 Latch Bit 4 SET Input (SELogic control equation)	S1SLT4	
Set 1 Latch Bit 4 RESET Input (SELogic control equation)	S1RLT4	
SELogic Control Equations Set 2		
Set 2 Variable 1 (SELogic control equation)	S2V1	These settings allow for the definitions of the SELogic control equations including their associated timer pickup and dropout times
S2V1 Timer Pickup (OFF, 0.000–999999.000 cycles)	S2V1PU	
S2V1 Timer Dropout (OFF, 0.000–999999.000 cycles)	S2V1DO	
Set 2 Variable 2 (SELogic control equation)	S2V2	
S2V2 Timer Pickup (OFF, 0.000–999999.000 cycles)	S2V2PU	
S2V2 Timer Dropout (OFF, 0.000–999999.000 cycles)	S2V2DO	
Set 2 Variable 3 (SELogic control equation)	S2V3	
S2V3 Timer Pickup (OFF, 0.000–999999.000 cycles)	S2V3PU	
S2V3 Timer Dropout (OFF, 0.000–999999.000 cycles)	S2V3DO	
Set 2 Variable 4 (SELogic control equation)	S2V4	
S2V4 Timer Pickup (OFF, 0.000–999999.000 cycles)	S2V4PU	
S2V4 Timer Dropout (OFF, 0.000–999999.000 cycles)	S2V4DO	
Set 2 Latch Bit 1 SET Input (SELogic control equation)	S2SLT1	These settings dictate the latch set and reset values for the SELogic equations defined above.
Set 2 Latch Bit 1 RESET Input (SELogic control equation)	S2RLT1	
Set 2 Latch Bit 2 SET Input (SELogic control equation)	S2SLT2	
Set 2 Latch Bit 2 RESET Input (SELogic control equation)	S2RLT2	
Set 2 Latch Bit 3 SET Input (SELogic control equation)	S2SLT3	
Set 2 Latch Bit 3 RESET Input (SELogic control equation)	S2RLT3	

Set 2 Latch Bit 4 SET Input (SELogic control equation)	S2SLT4	
Set 2 Latch Bit 4 RESET Input (SELogic control equation)	S2RLT4	
SELogic Control Equations Set 3		
Set 3 Variable 1 (SELogic control equation)	S3V1	These settings allow for the definitions of the SELogic control equations including their associated timer pickup and dropout times
S3V1 Timer Pickup (OFF, 0.000–999999.000 cycles)	S3V1PU	
S3V1 Timer Dropout (OFF, 0.000–999999.000 cycles)	S3V1DO	
Set 3 Variable 2 (SELogic control equation)	S3V2	
S3V2 Timer Pickup (OFF, 0.000–999999.000 cycles)	S3V2PU	
S3V2 Timer Dropout (OFF, 0.000–999999.000 cycles)	S3V2DO	
Set 3 Variable 3 (SELogic control equation)	S3V3	
S3V3 Timer Pickup (OFF, 0.000–999999.000 cycles)	S3V3PU	
S3V3 Timer Dropout (OFF, 0.000–999999.000 cycles)	S3V3DO	
Set 3 Variable 4 (SELogic control equation)	S3V4	
S3V4 Timer Pickup (OFF, 0.000–999999.000 cycles)	S3V4PU	
S3V4 Timer Dropout (OFF, 0.000–999999.000 cycles)	S3V4DO	
Set 3 Variable 5 (SELogic control equation)	S3V5	
S3V5 Timer Pickup (OFF, 0.000–999999.000 cycles)	S3V5PU	
S3V5 Timer Dropout (OFF, 0.000–999999.000 cycles)	S3V5DO	
Set 3 Variable 6 (SELogic control equation)	S3V6	
S3V6 Timer Pickup (OFF, 0.000–999999.000 cycles)	S3V6PU	
S3V6 Timer Dropout (OFF, 0.000–999999.000 cycles)	S3V6DO	
Set 3 Variable 7 (SELogic control equation)	S3V7	
S3V7 Timer Pickup (OFF, 0.000–999999.000 cycles)	S3V7PU	
S3V7 Timer Dropout (OFF, 0.000–999999.000 cycles)	S3V7DO	
Set 3 Variable 8 (SELogic control equation)	S3V8	
S3V8 Timer Pickup (OFF, 0.000–999999.000 cycles)	S3V8PU	
S3V8 Timer Dropout (OFF, 0.000–999999.000 cycles)	S3V8DO	
Set 3 Latch Bit 1 SET Input (SELogic control equation)	S3SLT1	These settings dictate the latch set and reset values for the SELogic equations defined above.
Set 3 Latch Bit 1 RESET Input (SELogic control equation)	S3RLT1	
Set 3 Latch Bit 2 SET Input (SELogic control equation)	S3SLT2	
Set 3 Latch Bit 2 RESET Input (SELogic control	S3RLT2	

equation)		
Set 3 Latch Bit 3 SET Input (SELogic control equation)	S3SLT3	
Set 3 Latch Bit 3 RESET Input (SELogic control equation)	S3RLT3	
Set 3 Latch Bit 4 SET Input (SELogic control equation)	S3SLT4	
Set 3 Latch Bit 4 RESET Input (SELogic control equation)	S3RLT4	
Set 3 Latch Bit 5 SET Input (SELogic control equation)	S3SLT5	
Set 3 Latch Bit 5 RESET Input (SELogic control equation)	S3RLT5	
Set 3 Latch Bit 6 SET Input (SELogic control equation)	S3SLT6	
Set 3 Latch Bit 6 RESET Input (SELogic control equation)	S3RLT6	
Set 3 Latch Bit 7 SET Input (SELogic control equation)	S3SLT7	
Set 3 Latch Bit 7 RESET Input (SELogic control equation)	S3RLT7	
Set 3 Latch Bit 8 SET Input (SELogic control equation)	S3SLT8	
Set 3 Latch Bit 8 RESET Input (SELogic control equation)	S3RLT8	
Trip Logic		
	TR1	Allows for an assignment of SELogic to control tripping of the circuit breaker
	TR2	
	TR3	
	TR4	
	TR5	
	ULTR1	Allows for the feedback of a successful trip latch and thus stopping the TRn signal from continuing
	ULTR2	
	ULTR3	
	ULTR4	
	ULTR5	
Close Logic		
	52A1	Dictates the circuit breaker state (open or closed)
	52A2	
	52A3	
	52A4	
	CL1	Allows for the setting of SELogic control equations for the resetting of the circuit breaker
	CL2	
	CL3	
	CL4	
	ULCL1	Allows for the feedback of a successful close of the circuit breaker and effectively unlatching the close logic
	ULCL2	
	ULCL3	
	ULCL4	
Event Report Triggering		

	ER	The SELogic equation to trigger an event report
Output Contact Logic (Standard Outputs)		
	OUT101	SELogic for configuring the outputs
	OUT102	
	OUT103	
	OUT104	
	OUT105	
	OUT106	
	OUT107	
Output Contact Logic (Extra Interface Board 2 or 6)		
	OUT201	SELogic for configuring the outputs (of the extra interface board)
	OUT202	
	OUT203	
	OUT204	
	OUT205	
	OUT206	
	OUT207	
	OUT208	
	OUT209	
	OUT210	
	OUT211	
	OUT212	
Output Contact Logic (Extra Interface Board 4)		
	OUT201	SELogic for configuring the outputs (of the extra interface board 4)
	OUT202	
	OUT203	
	OUT204	
Relay Settings		
Length of Event Report (15, 30, 60 cycles)	LER	Dictates the length of the Event report in cycles
Length of Pre-fault in Event Report (1 to 14 cycles)	PRE	Length of data of pre-fault conditions
Nominal Frequency (50, 60 Hz)	NFREQ	Sets the frequency of the system
Phase Rotation (ABC, ACB)	PHROT	Sets the phase rotation of the system
Date Format (MDY, YMD)	DATE_F	Sets the date format
Display Update Rate (1–60 seconds)	SCROLD	Sets the rate of the LCD display scroll rate
Front Panel Time-out (OFF, 0–30 minutes)	FP_TO	Sets the time that a menu or testing display will stay on the LCD screen before returning to the default screen display
Group Change Delay (0–900 seconds)	TGR	Dictates the time delay for settings groups to change between
RTDA Temperature Preference (C, F)	TMPREF A	Sets the temperature measurement (Fahrenheit or Degrees)
RTDB Temperature Preference (C, F)	TMPREF B	
Battery Monitor		
DC Battery Voltage Level 1 (OFF, 20–300 Vdc)	DC1P	Allows for setting of the DC battery

DC Battery Voltage Level 2 (OFF, 20–300 Vdc)	DC2P	voltages
DC Battery Voltage Level 3 (OFF, 20–300 Vdc)	DC3P	
DC Battery Voltage Level 4 (OFF, 20–300 Vdc)	DC4P	
Debounce Timers		
Input debounce time (0.00–2.00 cyc)	IN101D	Allows for the setting of the debounce times for each input.
Input debounce time (0.00–2.00 cyc)	IN102D	
Input debounce time (0.00–2.00 cyc)	IN103D	
Input debounce time (0.00–2.00 cyc)	IN104D	
Input debounce time (0.00–2.00 cyc)	IN105D	
Input debounce time (0.00–2.00 cyc)	IN106D	
Input debounce time (0.00–2.00 cyc)	IN201D	
Input debounce time (0.00–2.00 cyc)	IN202D	
Input debounce time (0.00–2.00 cyc)	IN203D	
Input debounce time (0.00–2.00 cyc)	IN204D	
Input debounce time (0.00–2.00 cyc)	IN205D	
Input debounce time (0.00–2.00 cyc)	IN206D	
Input debounce time (0.00–2.00 cyc)	IN207D	
Input debounce time (0.00–2.00 cyc)	IN208D	
Breaker 1 Monitor		
BKR1 Trigger Equation (SELogic control equation)	BKMON1	SELogic setting to allow for the initiation of the monitor
Close/Open Set Point 1 max (1–65000 operations)	B1COP1	Sets the minimum voltage open/close and the corresponding number of times that the breaker can be open/closed at this voltage
kA Interrupted Set Point 1 min (0.1–999.0 kA pri)	B1KAP1	
Close/Open Set Point 2 max (1–65000 operations)	B1COP2	Sets the middle curve voltage open/close and the corresponding number of times that the breaker can be open/closed at this voltage
kA Interrupted Set Point 2 min (0.1–999.0 kA pri)	B1KAP2	
Close/Open Set Point 3 max (1–65000 operations)	B1COP3	Sets the maximum voltage open/close and the corresponding number of times that the breaker can be open/closed at this voltage
kA Interrupted Set Point 3 min (0.1–999.0 kA pri)	B1KAP3	
Breaker 2 Monitor		
BKR2 Trigger Equation (SELogic control equation)	BKMON2	SELogic setting to allow for the initiation of the monitor
Close/Open Set Point 1 max (1–65000 operations)	B2COP1	Sets the minimum voltage open/close and the corresponding number of times that the breaker can be open/closed at this voltage
kA Interrupted Set Point 1 min (0.1–999.0 kA pri)	B2KAP1	
Close/Open Set Point 2 max (1–65000 operations)	B2COP2	Sets the middle curve voltage open/close and the corresponding number of times that the breaker can be open/closed at this voltage
kA Interrupted Set Point 2 min (0.1–999.0 kA pri)	B2KAP2	
Close/Open Set Point 3 max (1–65000 operations)	B2COP3	Sets the maximum voltage open/close and the corresponding number of times that the breaker can be open/closed at this voltage
kA Interrupted Set Point 3 min (0.1–999.0 kA pri)	B2KAP3	
Analog Input Labels		
Rename Current Input IAW1 (1–4 characters)	IAW1	Settings that allow for the renaming of the current inputs
Rename Current Input IBW1 (1–4 characters)	IBW1	

Rename Current Input ICW1 (1–4 characters)	ICW1	
Rename Current Input IAW2 (1–4 characters)	IAW2	
Rename Current Input IBW2 (1–4 characters)	IBW2	
Rename Current Input ICW2 (1–4 characters)	ICW2	
Rename Current Input IAW4 (1–4 characters)	IAW4 (IN1)	
Rename Current Input IBW4 (1–4 characters)	IBW4 (IN2)	
Rename Current Input ICW4 (1–4 characters)	ICW4 (IN3)	
Setting Group Selector		
Select Setting Group 1 (SELogic control equation)	SS1	SELogic equation for the determination of which setting group is to be used.
Select Setting Group 2 (SELogic control equation)	SS2	
Select Setting Group 3 (SELogic control equation)	SS3	
Select Setting Group 4 (SELogic control equation)	SS4	
Select Setting Group 5 (SELogic control equation)	SS5	
Select Setting Group 6 (SELogic control equation)	SS6	
Front Panel		
Energize LEDA (SELogic control equation)	LEDA =	These settings control what the LED front panel indicates. It also sets whether the LED is to be lit or not lit under those conditions.
Energize LEDB (SELogic control equation)	LEDB =	
Energize LEDC (SELogic control equation)	LEDC =	
Show Display Point 1 (SELogic control equation)	DP1 =	
DP1 Label 1 (16 characters) (Enter NA to Null)	DP1_1	
DP1 Label 0 (16 characters) (Enter NA to Null)	DP1_0	
Show Display Point 2 (SELogic control equation)	DP2 =	
DP2 Label 1 (16 characters) (Enter NA to Null)	DP2_1	
DP2 Label 0 (16 characters) (Enter NA to Null)	DP2_0	
Show Display Point 3 (SELogic control equation)	DP3 =	
DP3 Label 1 (16 characters) (Enter NA to Null)	DP3_1	
DP3 Label 0 (16 characters) (Enter NA to Null)	DP3_0	
Show Display Point 4 (SELogic control equation)	DP4 =	
DP4 Label 1 (16 characters) (Enter NA to Null)	DP4_1	
DP4 Label 0 (16 characters) (Enter NA to Null)	DP4_0	
Show Display Point 5 (SELogic control equation)	DP5 =	
DP5 Label 1 (16 characters) (Enter NA to Null)	DP5_1	
DP5 Label 0 (16 characters) (Enter NA to Null)	DP5_0	
Show Display Point 6 (SELogic control equation)	DP6 =	
DP6 Label 1 (16 characters) (Enter NA to Null)	DP6_1	
DP6 Label 0 (16 characters) (Enter NA to Null)	DP6_0	
Show Display Point 7 (SELogic control equation)	DP7 =	
DP7 Label 1 (16 characters) (Enter NA to Null)	DP7_1	
DP7 Label 0 (16 characters) (Enter NA to Null)	DP7_0	
Show Display Point 8 (SELogic control equation)	DP8 =	
DP8 Label 1 (16 characters) (Enter NA to Null)	DP8_1	
DP8 Label 0 (16 characters) (Enter NA to Null)	DP8_0	
Show Display Point 9 (SELogic control equation)	DP9 =	
DP9 Label 1 (16 characters) (Enter NA to Null)	DP9_1	

DP9 Label 0 (16 characters) (Enter NA to Null)	DP9_0	
Show Display Point 10 (SELogic control equation)	DP10 =	
DP10 Label 1 (16 characters) (Enter NA to Null)	DP10_1	
DP10 Label 0 (16 characters) (Enter NA to Null)	DP10_0	
Show Display Point 11 (SELogic control equation)	DP11 =	
DP11 Label 1 (16 characters) (Enter NA to Null)	DP11_1	
DP11 Label 0 (16 characters) (Enter NA to Null)	DP11_0	
Show Display Point 12 (SELogic control equation)	DP12 =	
DP12 Label 1 (16 characters) (Enter NA to Null)	DP12_1	
DP12 Label 0 (16 characters) (Enter NA to Null)	DP12_0	
Show Display Point 13 (SELogic control equation)	DP13 =	
DP13 Label 1 (16 characters) (Enter NA to Null)	DP13_1	
DP13 Label 0 (16 characters) (Enter NA to Null)	DP13_0	
Show Display Point 14 (SELogic control equation)	DP14 =	
DP14 Label 1 (16 characters) (Enter NA to Null)	DP14_1	
DP14 Label 0 (16 characters) (Enter NA to Null)	DP14_0	
Energize LED15 (SELogic control equation)	DP15 =	
Energize LED16 (SELogic control equation)	DP16 =	
Text Labels		
Local Bit LB1 Name (14 characters) (Enter NA to Null)	NLB1	Settings to control the locals bits. To name, clear and set the bits.
Clear Local Bit LB1 Label (7 characters) (Enter NA to Null)	CLB1	
Set Local Bit LB1 Label (7 characters) (Enter NA to Null)	SLB1	
Pulse Local Bit LB1 Label (7 characters) (Enter NA to Null)	PLB1	
Local Bit LB2 Name (14 characters) (Enter NA to Null)	NLB2	
Clear Local Bit LB2 Label (7 characters) (Enter NA to Null)	CLB2	
Set Local Bit LB2 Label (7 characters) (Enter NA to Null)	SLB2	
Pulse Local Bit LB2 Label (7 characters) (Enter NA to Null)	PLB2	
Local Bit LB3 Name (14 characters) (Enter NA to Null)	NLB3	
Clear Local Bit LB3 Label (7 characters) (Enter NA to Null)	CLB3	
Set Local Bit LB3 Label (7 characters) (Enter NA to Null)	SLB3	
Pulse Local Bit LB3 Label (7 characters) (Enter NA to Null)	PLB3	
Local Bit LB4 Name (14 characters) (Enter NA to Null)	NLB4	
Clear Local Bit LB4 Label (7 characters) (Enter NA to Null)	CLB4	
Set Local Bit LB4 Label (7 characters) (Enter NA to Null)	SLB4	
Pulse Local Bit LB4 Label (7 characters) (Enter NA to Null)	PLB4	

Local Bit LB5 Name (14 characters) (Enter NA to Null)	NLB5	
Clear Local Bit LB5 Label (7 characters) (Enter NA to Null)	CLB5	
Set Local Bit LB5 Label (7 characters) (Enter NA to Null)	SLB5	
Pulse Local Bit LB5 Label (7 characters) (Enter NA to Null)	PLB5	
Local Bit LB6 Name (14 characters) (Enter NA to Null)	NLB6	
Clear Local Bit LB6 Label (7 characters) (Enter NA to Null)	CLB6	
Set Local Bit LB6 Label (7 characters) (Enter NA to Null)	SLB6	
Pulse Local Bit LB6 Label (7 characters) (Enter NA to Null)	PLB6	
Local Bit LB7 Name (14 characters) (Enter NA to Null)	NLB7	
Clear Local Bit LB7 Label (7 characters) (Enter NA to Null)	CLB7	
Set Local Bit LB7 Label (7 characters) (Enter NA to Null)	SLB7	
Pulse Local Bit LB7 Label (7 characters) (Enter NA to Null)	PLB7	
Local Bit LB8 Name (14 characters) (Enter NA to Null)	NLB8	
Clear Local Bit LB8 Label (7 characters) (Enter NA to Null)	CLB8	
Set Local Bit LB8 Label (7 characters) (Enter NA to Null)	SLB8	
Pulse Local Bit LB8 Label (7 characters) (Enter NA to Null)	PLB8	
Local Bit LB9 Name (14 characters) (Enter NA to Null)	NLB9	
Clear Local Bit LB9 Label (7 characters) (Enter NA to Null)	CLB9	
Set Local Bit LB9 Label (7 characters) (Enter NA to Null)	SLB9	
Pulse Local Bit LB9 Label (7 characters) (Enter NA to Null)	PLB9	
Local Bit LB10 Name (14 characters) (Enter NA to Null)	NLB10	
Clear Local Bit LB10 Label (7 characters) (Enter NA to Null)	CLB10	
Set Local Bit LB10 Label (7 characters) (Enter NA to Null)	SLB10	
Pulse Local Bit LB10 Label (7 characters) (Enter NA to Null)	PLB10	
Local Bit LB11 Name (14 characters) (Enter NA to Null)	NLB11	
Clear Local Bit LB11 Label (7 characters) (Enter NA to Null)	CLB11	
Set Local Bit LB11 Label (7 characters) (Enter NA	SLB11	

to Null)		
Pulse Local Bit LB11 Label (7 characters) (Enter NA to Null)	PLB11	
Local Bit LB12 Name (14 characters) (Enter NA to Null)	NLB12	
Clear Local Bit LB12 Label (7 characters) (Enter NA to Null)	CLB12	
Set Local Bit LB12 Label (7 characters) (Enter NA to Null)	SLB12	
Pulse Local Bit LB12 Label (7 characters) (Enter NA to Null)	PLB12	
Local Bit LB13 Name (14 characters) (Enter NA to Null)	NLB13	
Clear Local Bit LB13 Label (7 characters) (Enter NA to Null)	CLB13	
Set Local Bit LB13 Label (7 characters) (Enter NA to Null)	SLB13	
Pulse Local Bit LB13 Label (7 characters) (Enter NA to Null)	PLB13	
Local Bit LB14 Name (14 characters) (Enter NA to Null)	NLB14	
Clear Local Bit LB14 Label (7 characters) (Enter NA to Null)	CLB14	
Set Local Bit LB14 Label (7 characters) (Enter NA to Null)	SLB14	
Pulse Local Bit LB14 Label (7 characters) (Enter NA to Null)	PLB14	
Local Bit LB15 Name (14 characters) (Enter NA to Null)	NLB15	
Clear Local Bit LB15 Label (7 characters) (Enter NA to Null)	CLB15	
Set Local Bit LB15 Label (7 characters) (Enter NA to Null)	SLB15	
Pulse Local Bit LB15 Label (7 characters) (Enter NA to Null)	PLB15	
Local Bit LB16 Name (14 characters) (Enter NA to Null)	NLB16	
Clear Local Bit LB16 Label (7 characters) (Enter NA to Null)	CLB16	
Set Local Bit LB16 Label (7 characters) (Enter NA to Null)	SLB16	
Pulse Local Bit LB16 Label (7 characters) (Enter NA to Null)	PLB16	
Trigger Conditions		
Trigger SER (24 Relay Word bits per SERn equation, 96 total)		
	SER1	Settings to determine what is to be included in SER event reports
	SER2	
	SER3	
	SER4	
Relay Word Bit Aliases		
Syntax: ‘Relay-Word Bit’ ‘Up to 15 characters’. Use NA to disable setting.		
	ALIAS1	Allows for the renaming of the Relay

	ALIAS2	word bits to be more user friendly and understandable
	ALIAS3	
	ALIAS4	
	ALIAS5	
	ALIAS6	
	ALIAS7	
	ALIAS8	
	ALIAS9	
	ALIAS10	
	ALIAS11	
	ALIAS12	
	ALIAS13	
	ALIAS14	
	ALIAS15	
	ALIAS16	
	ALIAS17	
	ALIAS18	
	ALIAS19	
	ALIAS20	
Port 1 (SET P 1) Rear Panel, EIA-485 plus IRIG-B		
Port Protocol (SEL, LMD, DNP, RTDA, RTDB)	PROTO	Settings to control the port
LMD Prefix (@, #, $, %, &)	PREFIX	
LMD Address (1–99)	ADDR	
LMD Settling Time (0.00–30.00 seconds)	SETTLE	
Baud (300, 1200, 2400, 4800, 9600, 19200)	SPEED	
Data Bits (7, 8)	BITS	
Parity Odd, Even, or None (O, E, N)	PARITY	
Stop Bits (1, 2)	STOP	
Time-out (for inactivity) (0–30 minutes)	T_OUT	
Send auto messages to port (Y, N)	AUTO	
Enable hardware handshaking (Y, N)	RTSCTS	
Fast Operate Enable (Y, N)	FASTOP	
Port 2 (SET P 2) Rear Panel, EIA-232 with IRIG-B		
Port Protocol (SEL, LMD, DNP, RTDA, RTDB)	PROTO	Settings to control the port
LMD Prefix (@, #, $, %, &)	PREFIX	
LMD Address (1–99)	ADDR	
LMD Settling Time (0.00–30.00 seconds)	SETTLE	
Baud (300, 1200, 2400, 4800, 9600, 19200)	SPEED	
Data Bits (7, 8)	BITS	
Parity Odd, Even, or None (O, E, N)	PARITY	
Stop Bits (1, 2)	STOP	
Time-out (for inactivity) (0–30 minutes)	T_OUT	
Send auto messages to port (Y, N)	AUTO	
Enable hardware handshaking (Y, N)	RTSCTS	
Fast Operate Enable (Y, N)	FASTOP	
Port 3 (SET P 3) Rear Panel, EIA-232		
Port Protocol (SEL, LMD, DNP, RTDA, RTDB)	PROTO	Settings to control the port

LMD Prefix (@, #, $, %, &)	PREFIX	
LMD Address (1–99)	ADDR	
LMD Settling Time (0.00–30.00 seconds)	SETTLE	
Baud (300, 1200, 2400, 4800, 9600, 19200)	SPEED	
Data Bits (7, 8)	BITS	
Parity Odd, Even, or None (O, E, N)	PARITY	
Stop Bits (1, 2)	STOP	
Time-out (for inactivity) (0–30 minutes)	T_OUT	
Send auto messages to port (Y, N)	AUTO	
Enable hardware handshaking (Y, N)	RTSCTS	
Fast Operate Enable (Y, N)	FASTOP	
Port 4 (SET P 4) Front Panel, EIA-232		
Port Protocol (SEL, LMD, DNP, RTDA, RTDB)	PROTO	Settings to control the port
LMD Prefix (@, #, $, %, &)	PREFIX	
LMD Address (1–99)	ADDR	
LMD Settling Time (0.00–30.00 seconds)	SETTLE	
Baud (300, 1200, 2400, 4800, 9600, 19200)	SPEED	
Data Bits (7, 8)	BITS	
Parity Odd, Even, or None (O, E, N)	PARITY	
Stop Bits (1, 2)	STOP	
Time-out (for inactivity) (0–30 minutes)	T_OUT	
Send auto messages to port (Y, N)	AUTO	
Enable hardware handshaking (Y, N)	RTSCTS	
Fast Operate Enable (Y, N)	FASTOP	
Port n (SET P n) Front Panel, EIA-232 for PROTO = RTDA		
Number of RTDA (0–12)	RTDNUMA	These settings control the type of module the RTD is. And to enable communication between the SEL-2600
RTD 1A Type (NA, PT100, NI100, NI120, CU10)	RTD1TA	
RTD 2A Type (NA, PT100, NI100, NI120, CU10)	RTD2TA	
RTD 3A Type (NA, PT100, NI100, NI120, CU10)	RTD3TA	
RTD 4A Type (NA, PT100, NI100, NI120, CU10)	RTD4TA	
RTD 5A Type (NA, PT100, NI100, NI120, CU10)	RTD5TA	
RTD 6A Type (NA, PT100, NI100, NI120, CU10)	RTD6TA	
RTD 7A Type (NA, PT100, NI100, NI120, CU10)	RTD7TA	
RTD 8A Type (NA, PT100, NI100, NI120, CU10)	RTD8TA	
RTD 9A Type (NA, PT100, NI100, NI120, CU10)	RTD9TA	
RTD 10A Type (NA, PT100, NI100, NI120, CU10)	RTD10TA	
RTD 11A Type (NA, PT100, NI100, NI120, CU10)	RTD11TA	
RTD 12A Type (NA, PT100, NI100, NI120, CU10)	RTD12TA	
Port n (SET P n) Front Panel, EIA-232 for PROTO = RTDB		
Number of RTDB (0–12)	RTDNUMB	These settings control the type of module the RTD is. And to enable communication between the SEL-2600
RTD 1B Type (NA, PT100, NI100, NI120, CU10)	RTD1TB	
RTD 2B Type (NA, PT100, NI100, NI120, CU10)	RTD2TB	
RTD 3B Type (NA, PT100, NI100, NI120, CU10)	RTD3TB	

RTD 4B Type (NA, PT100, NI100, NI120, CU10)	RTD4TB	
RTD 5B Type (NA, PT100, NI100, NI120, CU10)	RTD5TB	
RTD 6B Type (NA, PT100, NI100, NI120, CU10)	RTD6TB	
RTD 7B Type (NA, PT100, NI100, NI120, CU10)	RTD7TB	
RTD 8B Type (NA, PT100, NI100, NI120, CU10)	RTD8TB	
RTD 9B Type (NA, PT100, NI100, NI120, CU10)	RTD9TB	
RTD 10B Type (NA, PT100, NI100, NI120, CU10)	RTD10TB	
RTD 11B Type (NA, PT100, NI100, NI120, CU10)	RTD11TB	
RTD 12B Type (NA, PT100, NI100, NI120, CU10)	RTD12TB	

Table 1 - Explanation of the SEL-387A Relay Settings

4.3 Current System Settings

The test rack setup that incorporates the SEL-387A Differential Current relay needs to be configured according to those settings mentioned in table 1. The full settings sheets are detailed in Appendix B. These settings are current as of the 28 October 2008. These settings will be regarded as the default settings for that test rack composition until such time as a change to the rack occurs or a decision is made to alter a setting.

Inrush current has been allowed for through PCT2 and PCT4 being set to the threshold of 15%. This means that if the ratio of the second or fourth harmonic relative to the fundamental current, exceeds 15% the relay will not trip on a surge of current. Additionally there has been no use of the DC offset or harmonic restraint features of the SEL-387A relay.

CHAPTER 5: INRUSH CURRENT MATHEMATICAL MODELING

This chapter outlines the mathematics behind inrush current. Specifically it looks at the proof behind the second and fourth harmonics.

5.1 Mathematical Modeling Purpose

The purpose of mathematical modeling of a phenomenon is so that it can be understood better. Understanding how inrush current works and engages with the rest of the system allows for the integration of hardware or software that manages monitors and sometimes controls the impact that inrush current has on the system. By doing this, the system can be stabilized and therefore be improved.

5.2 Harmonics existing in inrush current

The current data from a Tektronix Digital Phosphor Oscilloscope at the energisation of the test rack transformer have been plotted in figure 9. It can be clearly seen that at energisation of the transformer, one phase spikes rapidly whilst the other two phases maintain normal waveforms. Unfortunately there is a significant amount of switch bounce in this example so the small initial period (approximately 100 samples or 4 milliseconds) is not a clear waveform.

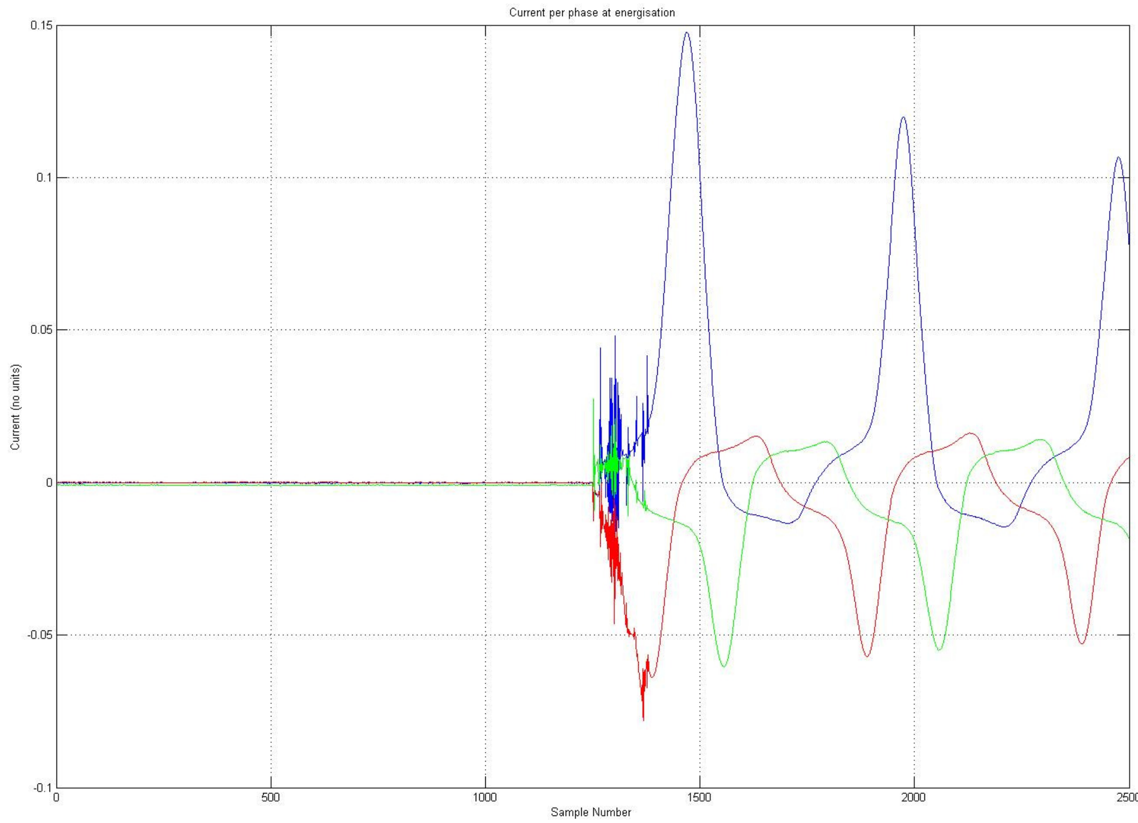

Figure 9 - Three Phase Energisation of a test transformer (Current)

From the data gathered, a Fast Fourier Transform (FFT) of the waveforms was conducted using MATLAB®. The full script for this transform is shown in Appendix C. The FFT was then plotted for each phase using a stem plot to show the relative magnitudes of each harmonic graphically. This graphic representation of the stem plot can be seen in Figure 10. It shows clearly that in each phase there are many harmonics. This is partly due to the shape of the steady state current waveform and partly due to the switch bounce noise at the energisation of the transformer. The plots show the first 25 harmonics and it is plain to see that the magnitudes of the later harmonics diminish to almost zero.

As expected, there are significant amounts of second harmonics. However the harmonic of most interest is the large 5^{th} harmonic (250Hz) in each phase. This is indicative of the switch bounce occurring at energisation of the transformer and is a problem in power systems due to damage caused through heat, circuit breaker tripping, fuse operation and possible equipment malfunction.

As part of future works, these current waveforms in Figure 9 will need to be filtered to determine the true representations of the harmonics.

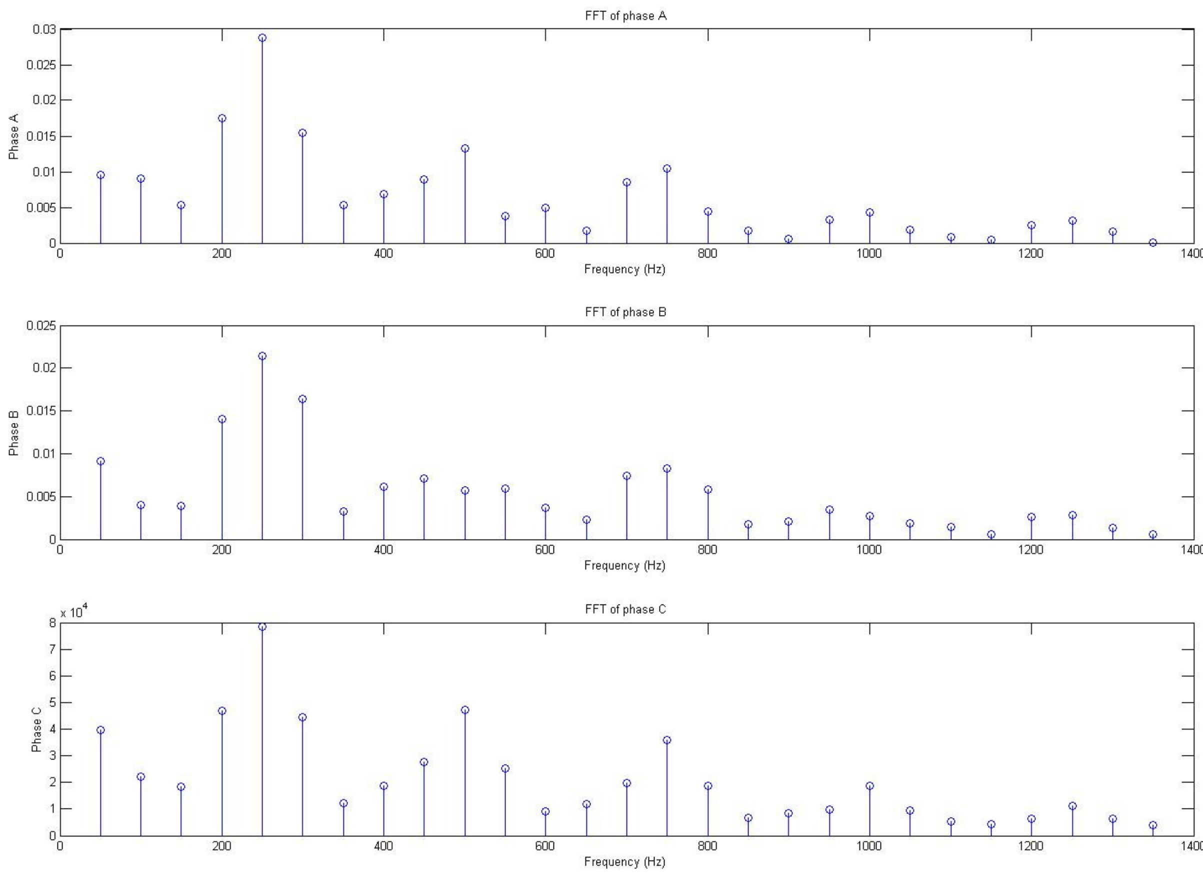

Figure 10 - Stem Plot of the harmonics in each phase

5.3 Differential relay discrimination against Inrush Current

The MATLAB® script described in section 5.2 is also used to calculate the 2nd harmonic ratio for each phase. This is utilsed as described in section 4.3, by the SEL-387A differential relay to set the relay's 2nd harmonic restraint. The calculated 2nd harmonic percentage ratios were:

Phase A = 94.78%

Phase B = 43.19%

Phase C = 55.97%

From these values, it is clear that the SEL-387A differential relay will not and did not trip due to the setting of 15% restraint.

CHAPTER 6: INRUSH CURRENT TEACHING PACKAGE

The purpose of this chapter is to provide material that will be suitable for inclusion into a power systems protection course or as a stand alone short course. This chapter details what inrush current is, how to set up a test rack for inrush current testing and also how to connect the rack to ensure the compatibility with SCADA and the PLC. Finally there will be review questions.

It is important to note here that the inrush current theory shown in this chapter is not new to this dissertation. The material covered is to be used as a teaching course and reiterates most of the theoretical components already covered.

6.1 Inrush Current Theory

Inrush current is a phenomenon that has been known of since transformers were first created over 200 years ago. Many of the mathematical understandings and methods of controlling the effects of inrush current have been modified and refined for the entirety of that period. Inrush current has also been referred to as magnetizing current, surge current, magnetizing inrush and input surge current.

Figure 11 shows a simple transformer diagram of the primary windings (i.e. no load). In the diagram, v represents the voltage of EMF of the windings, i represents the primary side current, N represents the number of turns (of the windings) and x is a switch.

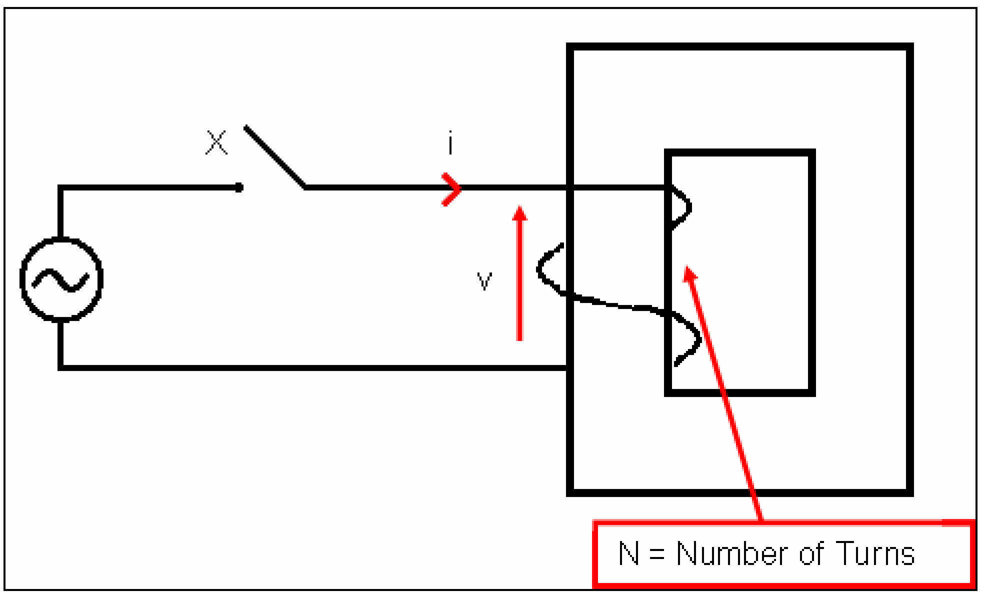

Figure 11 - Transformer Model No-Load

For this transformer model it is known that the voltage, V is directly proportional to the Number turns by the change in magnetic flux over the change in time. As represented by the below formula.

$$V = N\frac{\partial \phi}{\partial t}$$

Where magnetic flux is represented by phi = Φ, number of turns =N, voltage=V and the time =t.

This model demonstrates that at steady state (i.e. when the transformer is operating under normal conditions after a long continuous period) that the voltage and magnetic flux are directly proportional. Subsequently the voltage and the current are also directly proportional. This can be shown as a representation of two waveforms, a voltage waveform and a magnetic flux waveform. Where Voltage=Sin(ωt) and Magnetic Flux=Cos(ωt) and is seen in figure 12.

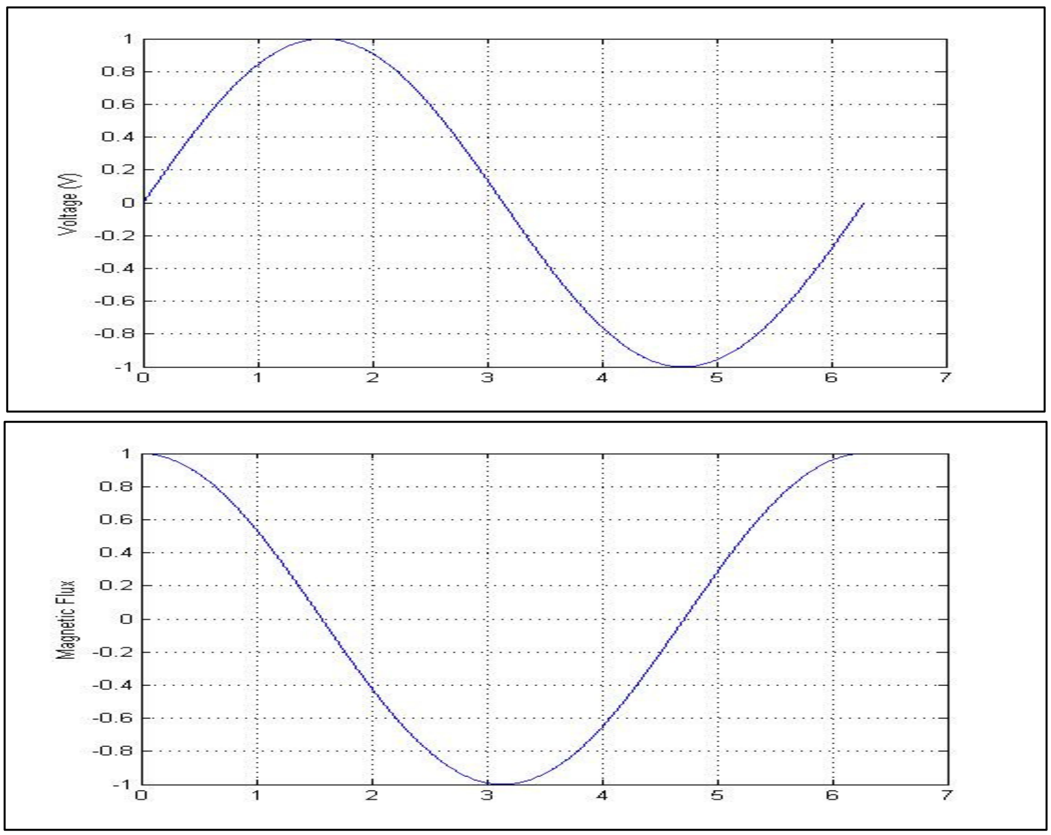

Figure 12 - Steady State Voltage and Magnetic Flux Waveforms

Using Ohm's law, current can be calculated by using the number of turns and the magnetic flux so that current becomes proportional to NΦ as per the below formula.

$$i \propto N\Phi$$

This relationship in a perfect situation would behave in a linear fashion. However the real relationship between current and magnetic flux is in a hysterisis loop arrangement. A real hysterisis loop of a test transformer at the University of Southern Queensland, performed by Dr Tony Ahfock, can be seen in figure 13. This diagram shows that the magnetic flux versus the current in a transformer does not follow a linear relationship but rather forms an envelope, hysterisis arrangement. It can also be seen that when the flux is very high, current can be tending towards infinitely high (shown by the flat line at the top of the hysterisis loop).

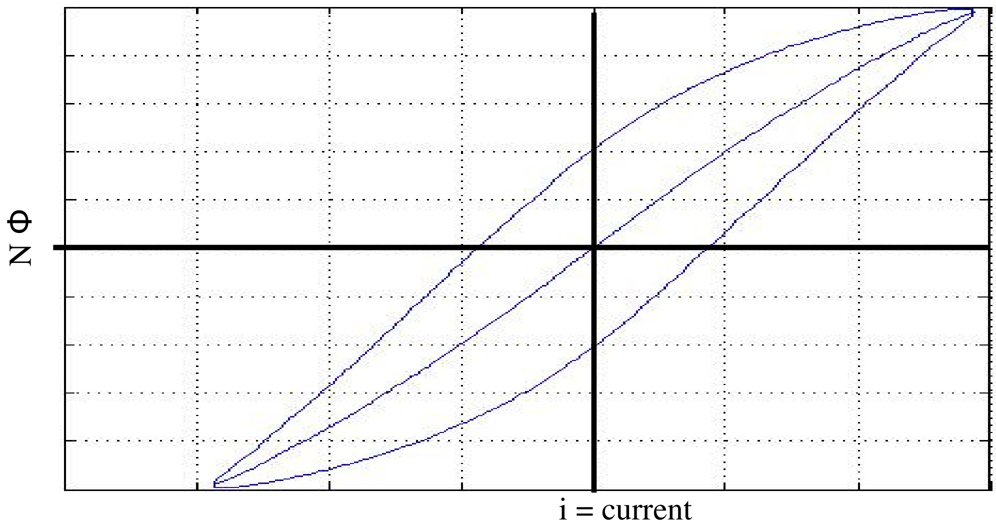

Figure 13 - Transformer Hysterisis Loop

Dr Tony Ahfock (USQ), along with students, has performed many tests on single and three phase transformers analyzing the inrush current phenomenon. Figure 14 shows one such energisation. It can be seen in the diagram that the transformer has voltage applied to the primary side at approximately 0.052 seconds. It can also be seen that the time at which the voltage is applied to the transformer is almost half way through one cycle of the AC voltage waveform. The applied voltage is approximately 600Vpeak.

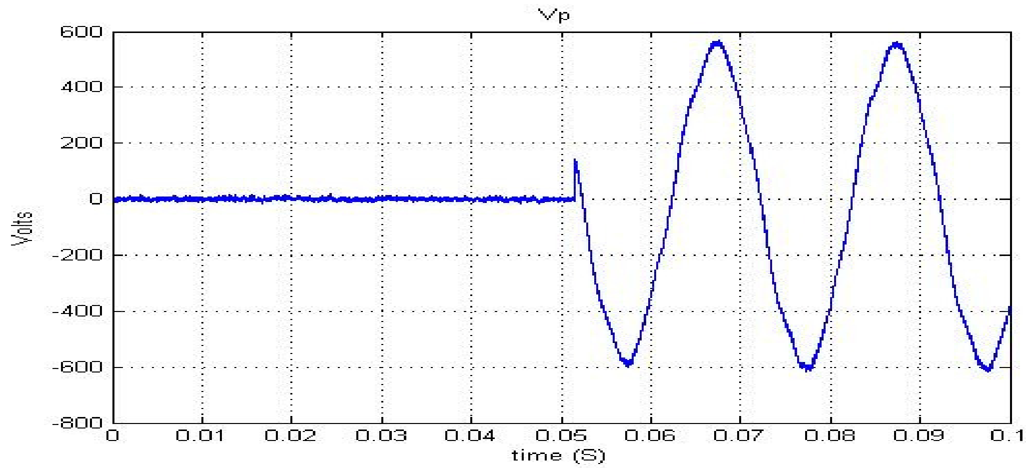

Figure 14 - Voltage Applied to Primary Side of Transformer

The corresponding current waveform is shown in figure 15. In this diagram, two clear decaying peaks can be seen, with a third slightly obscured. The diagram also shows the current drawn reaches approximately 150A which is well above the rated current of this transformer. The first peak is delayed by approximately 0.01 seconds due to the lagging nature of the current. If this waveform was run till steady state, a smooth cosine shaped curve centered about the x-axis would be visible.

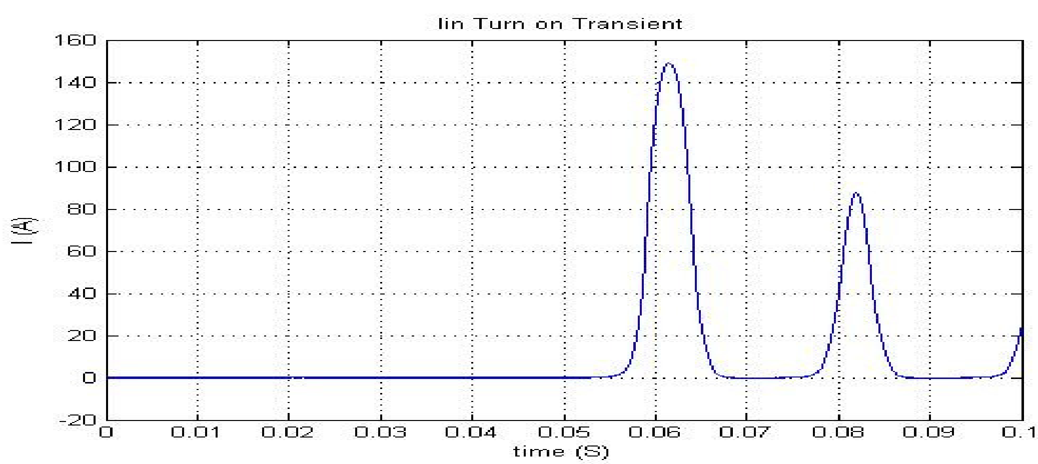

Figure 15 - Current Response to Input Voltage

6.2 PLC and SCADA set up

This test rack set up utilises PLC and SCADA functionality so that it can be controlled remotely. The PLC ladder diagram, as shown in figure 16, is the logic for the operation of the circuit breakers for the test rack system. Within this test rack system the circuit breakers are standard coil controlled contactors as the operating conditions of the test rack are a scaled version of a real system.

The SCADA interface allows a user to control the test rack system from a remote location via the internet. The SCADA interface, as seen in figure 17, accepts control of the system breakers either side of the entire system, the transformer breakers either side of the transformer and also allows for the application of faults to the neutral of the transformer (ground fault) and also line to line faults at the load. For the purposes of inrush demonstration the focus will be primarily on the Circuit Breaker “0” and circuit breaker “1”.

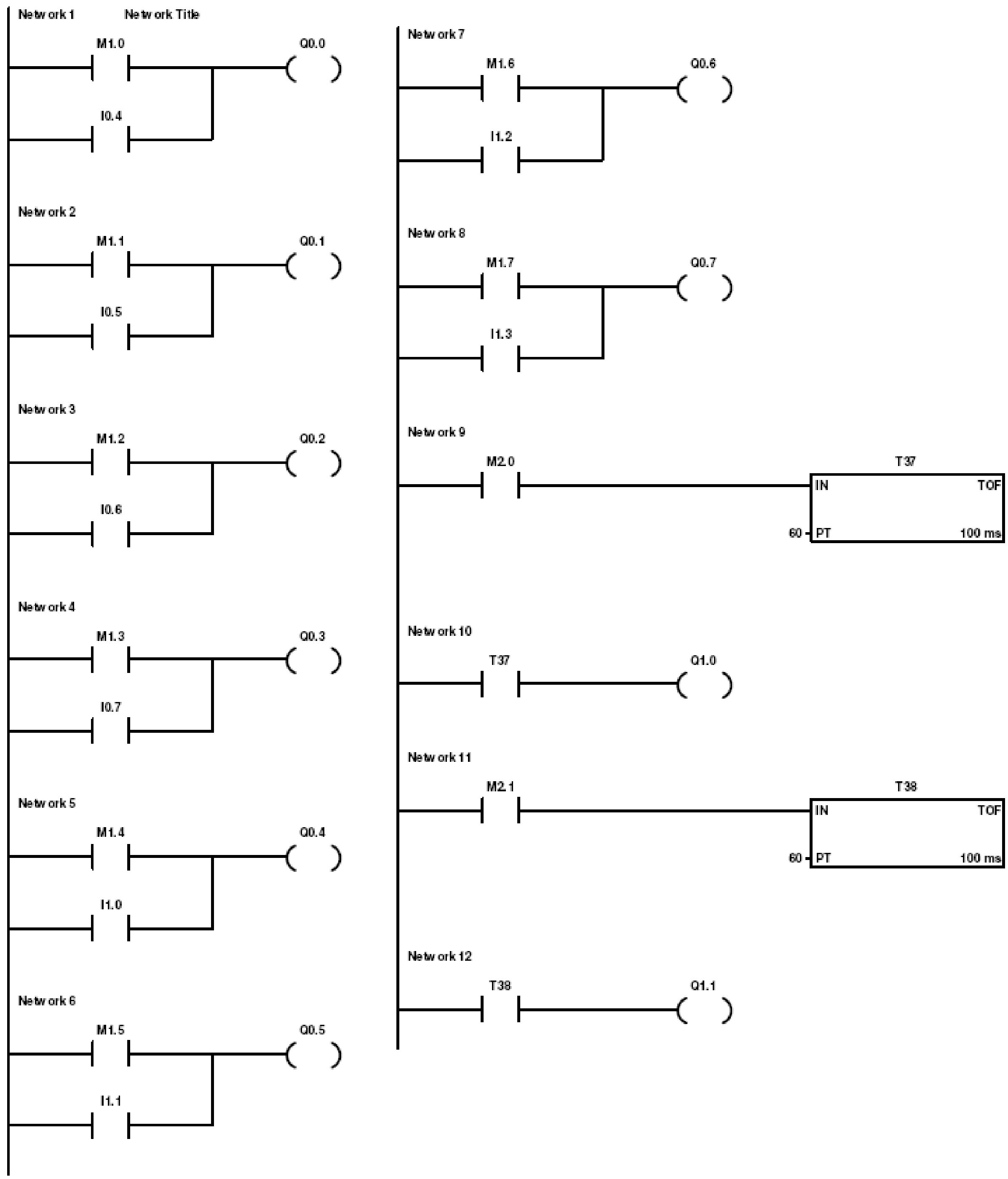

Figure 16 - PLC Ladder Diagram for the Circuit Breaker

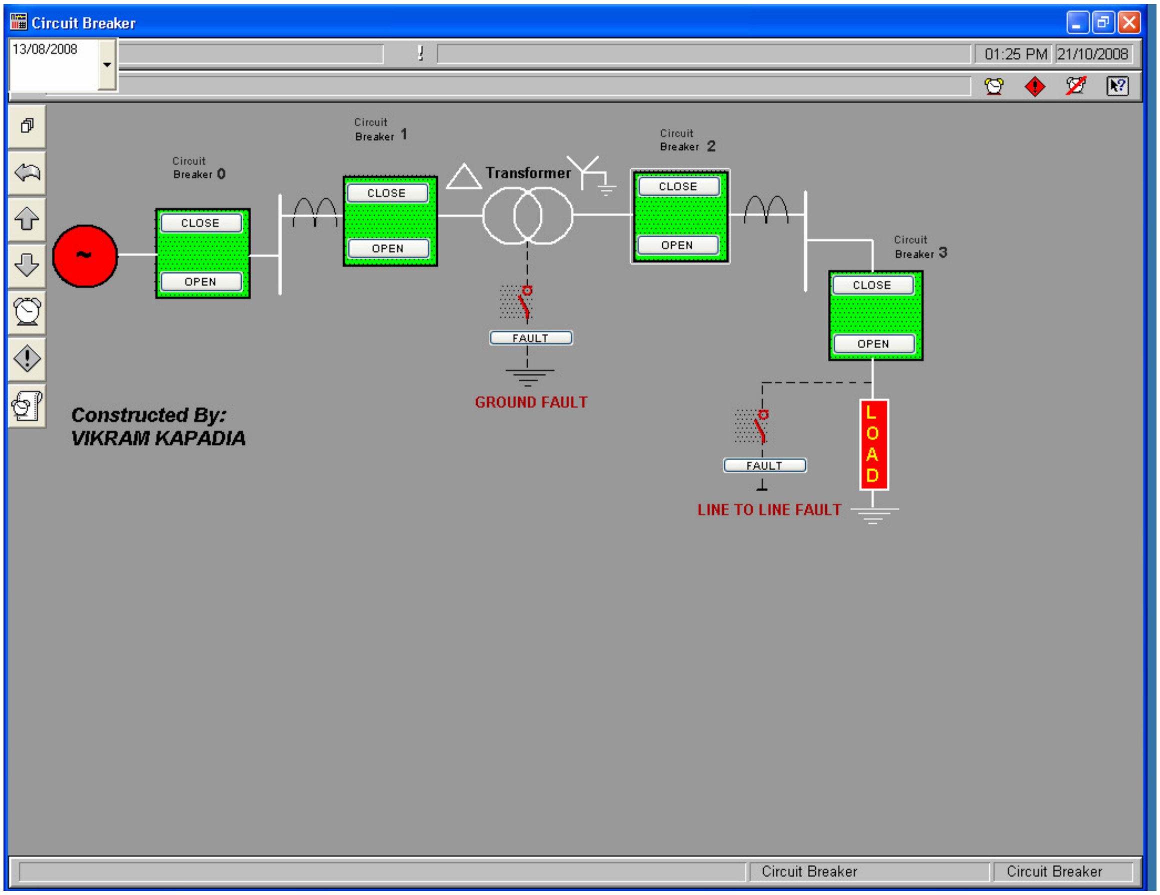

Figure 17 - SCADA interface to the test rack system

6.3 Test Rack Setup for Inrush Current observation

Figure 18 shows the links between the components of the test rack set up. It can be seen that the circuit breakers are controlled via both the Siemens S7-200 PLC and also through the SEL-387A relay and both are configured via the computer terminal. As described earlier, the circuit breakers (top shaded box) are in fact two contactors within the test rack facility. The transformer that will undergo analyse is also within the test rack facility and is connected as shown in the schematic (right shaded box), with the current probes detecting the current on each phase. The oscilloscope that will be used is the Tektronix TDS5034B Digital Phosphor Oscilloscope due to its ability to be accessed remotely and so that data can be collected digitally for analysis.

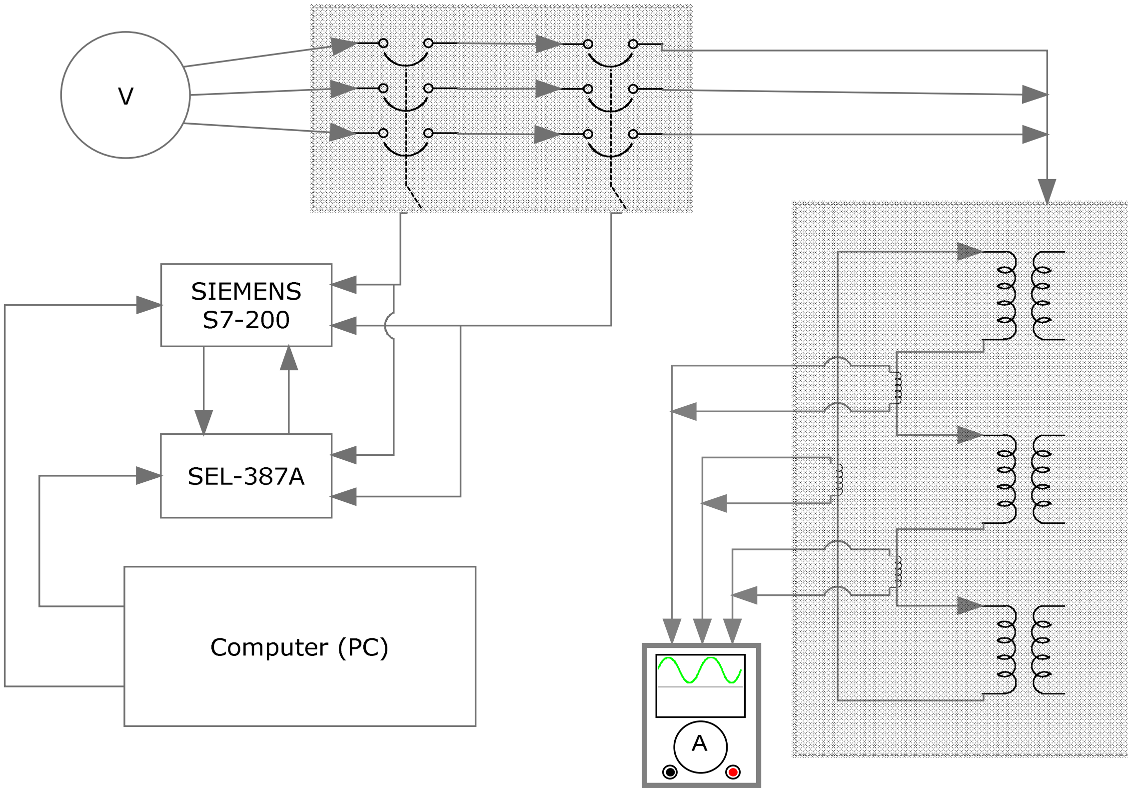

Figure 18 - Test Rack design

6.4 Inrush Current Observation Activity

Equipment Required:

- Tektronix TDS503B Digital Phosphor Oscilloscope
- 3x Tektronix TCP202 Current Probes
- Faultable Transformer (Test Rack)
- Contactors (Test Rack)
- SEL-387A
- Siemens S7-200
- Computer Running "CITECT Explorer"
- Enough leads to connect the system

SAFETY NOTICE

High voltages and currents are present in this observation activity! Practice safe work habits by following this checklist.

- **Ensure that all leads are in good conditions**
- **Ensure leads are suitably rated for the expected currents**
- **Ensure that power is switched off when changing or altering the leads on the test rack**
- **Wear applicable personal protective equipment (PPE)**
- **Get the test rack connections checked by a supervisor before powering up**

Failing to comply with any one of these requirements could result in electrocution and possibly death

STEP 1 – Test Rack set up

Connect up the test rack, PLC and SEL-387A as per the schematic. Connect the Current Probes to the Oscilloscope and then, ensuring correct direction of the probe, attach them to the transformer also like the schematic.

STEP 2 – SCADA setup

Power up the PC, Oscilloscope and the PLC; once the PC has booted up and logged in open “CITECT explorer” and follow the action path below.

> Select Circuit Breaker (from the available SCADA files) > File > Run (wait for the configuration to complete) > Pages > Circuit Breaker.

You should now see the SCADA circuit Breaker interface as seen in figure 17.

STEP 3 – Oscilloscope Configuration

The oscilloscope should now be running and there should be waveforms on the screen. Degauss each of the current probes and centre each of them using the wheel on the probe and also on oscilloscope.

Power up the test rack. On the SCADA interface select CLOSE for circuit breaker 0 and also for circuit breaker 1. There should now be a waveform for each of the current probes, change the scale so that this waveform on takes up two (2) increments centered about the middle of the scope window.

On the SCADA interface now select the OPEN for circuit breaker 1 and then for circuit breaker 0.

STEP 4 – Inrush observation

You are now ready to observe the inrush current phenomenon.

Prepare the oscilloscope by hitting the RUN/STOP button, the SINGLE button and then the RUN/STOP button again until the counter in the middle top of the window is incrementing.

On the SCADA window select CLOSE on circuit breaker 0 and then select CLOSE on circuit breaker 1. You will notice a lot of distortion and then the oscilloscope will show a steady waveform on each of the channels.

Now press the SINGLE button.

STEP 5 – Data collection

Click File>Save As from the menu

Select Waveform Options from the sidebar and select the channel that the first probe is connected to and also changing the data type to CSV (Comma separated Variable) select Ok. Then save this file as "Phase A" to a USB thumb drive

Repeat this process for each channel ensuring that each channel is named differently.

STEP 6 – Power down

On the SCADA interface now select the OPEN for circuit breaker 1 and then for circuit breaker 0.

Close the "CITECT explorer" window and turn off the PLC and Test Rack.

STEP 7 – Data Manipulation

Using the MATLAB® script provided in Appendix C, rename the files to match the required Matlab input and save them in the same directory. Change the working directory of MATLAB® and run the file.

The output of the file will show a plot of the current in each phase, if this plot shows the currents not centered, then adjust by adding or subtracting the offset in the Matlab script until centered. The second plot will be the harmonic subplots for each phase.

6.5 Summary and Conclusions

This observation exercise has taught you about the phenomenon of inrush current. It has shown you how to set up test equipment, to measure current and to use a SCADA interface. It also has shown that there is a link between PLC programming and remote access through SCADA.

In regard to inrush current you have learnt that the magnitude of inrush current is dependant on the magnetic flux. Because of this relationship, the inrush current magnitude is random. You have also seen that the inrush current will never occur on all three phases. Additionally you have observed that inrush current is far in excess of the steady state current of the transformer.

6.6 Review Questions and Answers

These questions are designed to test your knowledge of inrush current and also to provide the stimulus to research the causes and conventional fixes to the phenomenon.

Question 1

What are the causes of inrush current?

Question 2

What are some of consequences of inrush current?

Question 3

What things can be done to minimise the magnitude of Inrush current?

Question 4

From observing inrush current, does Inrush current present on all three phases?

Question 5

From observation of inrush current, are there sizeable second harmonics present in the inrush current?

Question 6

What changes will be observed if this experiment was performed multiple times?

Answer 1

Inrush current is caused by the residual flux in a transformer coupled with the application of a voltage to the transformer.

Answer 2

- Large mechanical stresses
- Tripping of transformer protection devices (nuisance tripping)
- Heat
- Energy loss
- Large current draw

Answer 3

- Controlled switching
- Application of Thermistors
- Allowing all the residual flux to dissipate

Answer 4

Commonly, No. however there is often switch bounce distortion on the other phases that is mistaken as inrush current 2^{nd} and 4^{th} harmonics.

Answer 5

Yes

Answer 6

- The phase that the inrush current spike occurs will change
- The magnitude of inrush current will change
- The time for the inrush current to settle will change

CHAPTER 7: FUTURE WORKS

This chapter outlines the works that could be undertaken to expand on the works already covered in this dissertation. It also outlines the advantages of undertaking those works for the benefit of Engineering and the University of Southern Queensland.

7.1 Future Works to be undertaken

Whilst working through this project several areas of future works have been determined to be beneficial.

This first and primary future works that need to be undertaken is the design of a Matlab® filter to "clean" the waveforms that are produced by the Tektronix Oscilloscope. This will reduce the switch bounce noise and provide more accurate harmonic magnitudes.

The second area is in the designing and building of more additions to the test rack facility. Specifically more work can be done in the incorporation of a feeder protection relay into the construction of the test rack. This will allow students at the University of Southern Queensland to have access to a modeled substation that can be controlled through SCADA.

The third area is expanding of the teaching package that has been developed for inrush current. The areas of expansion include Restricted Earth Fault (REF), Over Current (OC) and Sensitive Earth Fault (SEF). This will provide a more comprehensive learning package for students interested in protection of power systems.

The incorporation of an autoreclose (AR) facility into the test rack is another area of future works. This will provide a practical example of how certain faults are handled in a real power system. The autoreclose process could be incorporated either as software utilising the SEL-387A current differential relay or through a commercially available recloser such as the Nulec.

Another area of future works is developing the remoteness of the test rack. Unfortunately this project was unable to provide a fully working remote test rack due to complications with the SEL-387A relay functionalities. This could be overcome through setting manipulation and event recording tweaking. Alternatively providing the Tektronics oscilloscope through SCADA will also solve the remoteness issues.

Finally the last area that has been established as a future works need is the mathematical modeling of inrush current. As a part of this project research has been conducted into the mathematics of inrush current magnitude prediction and calculation. From that research it is clear that there are numerous models that all take into effect different factors. Future project options could be the development of these

7.2 Advantages of Future Works

If the future works described in Section 7.1 are undertaken there are beneficial outcomes to the University of Southern Queensland and also to the students that attend there.

The University will be positively affected by the creation of a robust, industry standard test rack facility that can simulate the operation of faults in a normal power substation. This sort of equipment, if accessible by external students through SCADA, will provide USQ with the hardware needed to compete with other institutions for the students requiring post-graduate or undergraduate courses in protection systems. This will not only draw funds to the University by companies such as Ergon and Energex but will also increase the reputation USQ has as a provider of quality distance education courses.

The students (present and future) will benefit because they will have access to the resources they need to understand and succeed in the study of power protection systems. This will increase their job readiness for the power profession.

CHAPTER 8: SUMMARY AND CONCLUSIONS

This chapter outlines the conclusions made from this project and subsequent dissertation. It also covers the completeness of the project specification as detailed in Appendix A.

8.1 Summary of Achievements

The aims and objective set out at the beginning of the project as listed in Appendix A were:

1. Research Inrush Current test characteristics of Power Transformers
2. Discuss with Industry Professionals and Academics, the main features that are to be included in a transformer Inrush Current test facility.
3. Design and build a transformer Inrush Current Test rack that can be PLC controlled
4. Program the PLC to conduct all Inrush Current test requirements including the use of protection relays
5. Design and create the SCADA interface for the PLC and Inrush Current test environment
6. Write full documentation on the design and operation the of the equipment suitable for use as a teaching course
7. Develop and validate mathematical models to explain transformer inrush current
8. Complete dissertation

Objective one and two were maintained throughout the course of the project year. It included conducting research into not only on inrush current but also into power quality, Matlab FFT scripting and also data acquisitions techniques. The discussion with industry professionals was mostly carried out by Dr Tony Ahfock and the requirements of industry were passed back in meeting with him.

Objective three through to five were all hijacked throughout the project year by other student and lecturers at USQ completing parallel studies. Bob Burgess has completed a significant amount of work in test rack configuration and design whilst Vikram Kapadia has created the SCADA and PLC programming that have been utilised in this course. However in preparing for these objectives the tutorials for both the PLC and SCADA programming were completed. Additionally the understanding of the set up of the SCADA, PLC and test rack were all vital for the successful data acquisition within this project.

Objectives six and eight were undertaken as part of this final presentation. As can be seen from the previous seven chapters they have been completed in full.

Objective seven has been not completed to the fullness as anticipated at the start of this project. It was initially anticipated that the mathematical model would include studies into the three phase magnetizing flux. However due to time restrictions and external complications this area of study was molded into a study of the harmonics present in the inrush current waveform. As described in the future works chapter, this will also need to be refined and modeled due to the complications of the switch bounce in the contactors.

8.2 Conclusion

This project aimed to provide a remotely accessible testing facility for remote inrush testing of power transformers. Although the objectives were not completed to the full, the overall objective of understanding the setup of the test rack and the setting of the SEL-387A relay will be of utmost importance to future students and academics using these facilities. It has also been confirmed that rich second harmonics exist in the inrush current drawn by the transformer at energisation as shown by the FFT.

REFERENCES

Ametherm, 2008, available at URL: http://www.ametherm.com/Inrush_Current/inrush_current_faq.html Accessed 20/10/08

M. Stuerer, K. Frohlich, 2002, "The Impact of Inrush Currents on the Mechanical Stress of High Voltage Power Transformer Coils", Transactions on Power Delivery, Vol. 17, No. 1 January, pp155-160

A. Ahfock, A. Hewitt, 2006, "DC Magnetization of Transformers", IEEE Power Applications, Vol. 153, No. 4, July 2006, pp601-607

K. Basu, A. Asghar, S. Morris, 2006, "Effect of Sequential Phase Energisation on the Inrush Current of a Delta Connected Transformer", IEEE

R. Hunt, J. Shaefer, B. Bentert, 2008, "Practical Experience in Setting Transformer Differential Inrush Restraint", IEEE

S. Hong, W. Qin, 2000, "A wavelet-based method to discriminate between Inrush Current and Internal Fault", IEEE

BIBLIOGRAPHY

University of Southern Queensland, 2004, “ELE1911 Electrical and Electronic Practice A - Energy Systems Laboratory: Safety Rules”, University of Southern Queensland, Toowoomba, Qld, Australia

Heathcote, Martin (1998-11-03). J & P Transformer Book, Twelfth edition. Newnes, pp. 2–3

National Energy Information Centre (NEIC), 2004, Available at URL: http://www.eia.doe.gov/oiaf/1605/ggccebro/chapter1.html Accessed: 24 May 2008

S. Hong, W. Qin, 2000, “A wavelet-based method to discriminate between Inrush Current and Internal Fault”, IEEE

R. Girgis, E. teNyenhuis, 2007, “Characteristics of Inrush Current of Present Designs of Power Transformers”, IEEE

M. Stuerer, K. Frohlich, 2002, “The Impact of Inrush Currents on the Mechanical Stress of High Voltage Power Transformer Coils”, Transactions on Power Delivery, Vol. 17, No. 1 January, pp155-160

R. Hunt, J. Shaefer, B. Bentert, 2008, “Practical Experience in Setting Transformer Differential Inrush Restraint”, IEEE

B. Kasztenny, 2008, “Impact of Transformer Inrush Currents on Sensitive Protection Functions, How to Configure Adjacent Relays to Avoid Nuisance Tripping?”, Proceedings of the 59th Annual Conference for Protective Relay Engineers, pp103-123

D. Zhang, H. Yang, G. Yu, X. Wang, W. Wang, 2006, “Correlation Analysis of Waveforms in Non-Saturation Zone Based Method to Identify the Magnetising Inrush in Transformer”, Proceedings from 2006 International Conference on Power System Technology

J. Boys, C. Chen, G. Covic, Date Unknown, “Controlling Inrush Currents in Inductively Coupled Power Systems”, IEEE

K. Basu, A. Asghar, S. Morris, 2006, “Effect of Sequential Phase Energisation on the Inrush Current of a Delta Connected Transformer”, IEEE

D. Bi, X. Zhang, H. Yang, G. Yu, X. Wang, W. Wang, 2007, “Correlation Analysis of Waveforms in Nonsaturation Zone-Based Method to identify the Magnetizing Inrush Transformer”, Proceedings of IEEE Transactions on Power Delivery, Vol. 22, No.3, July 2007, pp1380-1385

P. Cheng, W. Chen, Y. Chen, C. Ni, J. Lin, 2007, “A Transformer Inrush Mitigation Method for Series voltage Sag Compensators”, From the Proceedings of IEEE Transactions on Power Electronics, Vol. 22, No. 5, September 2007, pp1890-1899

S. Chen, R. Lin, C. Cheng, 2005, “Magnetizing Inrush Model of Transformers Based on Structure Parameters”, Proceedings of IEEE Transactions on Power Delivery, Vol. 20, No. 3, July 2005, pp1947-1954

A. Ahfock, A. Hewitt, 2006, “DC Magnetization of Transformers”, IEEE Power Applications, Vol. 153, No. 4, July 2006, pp601-607

J. Grainger, W. Stevenson Jr., 1994, “Power Systems Analysis”, McGraw Hill Inc, United States of America

R. Girgis, 2001, “Inrush Current Tutorial Session”, IEEE Standards Conference Orlando Florida Oct 15, 2001.

J. Oliveira, C. Tavares, 2006, “Transformer Controlled Switching to Eliminate Inrush Current – Part I: Theory and Laboratory Validation”, IEEE Xplore Downloaded 20 October, 2008

J Brunke, K Frohlich, 2001, “Elimination of Transformer Inrush Currents by Controlled Switching – Part I: Theoretical Consideration”, IEEE Transactions on Power Delivery, Vol 16, No 2, April 2001

J Brunke, K Frohlich, 2001, “Elimination of Transformer Inrush Currents by Controlled Switching – Part II: Application Performance Consideration”, IEEE Transactions on Power Delivery, Vol 16, No 2, April 2001

K Yabe, 1997, Power Differential Method for Discrimination between fault and magnetizing Inrush Current in transformers”, IEEE Transactions on Power Delivery, Vol. 12, No. 3, July 1997

A. Eltom, R. Harnshotipun, 2002, “Microprocessor-based relay laboratory with industry support, IEEE

S. Abdulsalem, W. Xu, 2005, “Analytical study of Transformer Inrush Current Transients and its applications”, International Conference on Power Systems Transients, Montreal Canada, June 19-23, 2005.

Y. Wang, S. Adbulsalem, W. Xu, 2008, “Analytical Formula to Estimate the Maximum Inrush Current”, IEEE Transactions on power delivery, Vol. 23, No. 2, April 2008

H. Bronzeado, S. Pinto, P Jonsson, J. Carlos, M. Chaves, “Transformer Controlled Switching to Eliminate Inrush Current – Part II: Field Tests on a 100MVA Three Phase

Transformer", 2006 IEEE PES Transmission and Distribution Conference and Exposition Latin America, Venezuela

APPENDICES

Appendix A- Project Specification

University of Southern Queensland
FACULTY OF ENGINEERING AND SURVEYING

ENG4111/4112 Research Project
PROJECT SPECIFICATION

FOR: GLENN WILLIAM **SPRINGALL**

TOPIC: DESIGN AND IMPLEMENTATION OF A REMOTELY ACCESSIBLE TESTING FACILITY FOR POWER (DISTRIBUTION) TRANSFORMERS

SUPERVISOR: Dr Tony Ahfock

PROJECT AIM: To implement an internet accessible testing facility to surge test power transformers at 25kVA. The project will consist of creating a PLC controlled device with a SCADA interface.

PROGRAMME: *Issue A, 17 March 2008*

9. Research Inrush Current test characteristics of Power Transformers
10. Discuss with Industry Professionals and Academics, the main features that are to be included in a transformer Inrush Current test facility.
11. Design and build a transformer Inrush Current Test rack that can be PLC controlled
12. Program the PLC to conduct all Inrush Current test requirements including the use of protection relays
13. Design and create the SCADA interface for the PLC and Inrush Current test environment
14. Write full documentation on the design and operation the of the equipment suitable for use as a teaching course
15. Develop and validate mathematical models to explain transformer inrush current
16. Complete dissertation

AGREED:

___________________ (Student) Date: ___/___/2008

___________________ (Supervisor) Date: ___/___/2008

Appendix B- Relay Setting Sheets for the SEL-387A as at 28 October 2008

Configuration Settings
Relay Identifier (39 Characters)
RID = XFMR 1 S/N 2008049229
Terminal Identifier (59 Characters)
TID = STATION A

Enable Differential Element (Y, N)	E87	=	Y
Enable Winding 1 O/C Elements and Dmd Thresholds (Y, N)	EOC1	=	N
Enable Winding 2 O/C Elements and Dmd Thresholds (Y, N)	EOC2	=	N
Enable Winding Neutral Elements (Y, N)	EOCN	=	N
Enable RTDA Element (Y, N)	E49A	=	N
Enable RTDB Element (Y, N)	E49B	=	N
Enable SELogic® Control Equations Set 1 (Y, N)	ESLS1	=	N
Enable SELogic Control Equations Set 2 (Y, N)	ESLS2	=	N
Enable SELogic Control Equations Set 3 (Y, N)	ESLS3	=	N

General Data

Winding 1 CT Connection (D, Y)	W1CT	=	Y
Winding 2 CT Connection (D, Y)	W2CT	=	Y
Winding 1 CT Ratio (1–50000)	CTR1	=	20
Winding 2 CT Ratio (1–50000)	CTR2	=	120
Neutral 1 CT Ratio (1–50000)	CTRN1	=	120
Neutral 2 CT Ratio (1–50000)	CTRN2	=	120
Neutral 3 CT Ratio (1–50000)	CTRN3	=	120
Maximum Power Xfmr Capacity (OFF, 0.2–5000.0 MVA)	MVA	=	12.0
Define Internal CT Connection Compensation (Y, N)	ICOM	=	Y
Winding 1 CT Conn. Compensation (0, 1, …, 12)	W1CTC	=	12
Winding 2 CT Conn. Compensation (0, 1, …, 12)	W2CTC	=	YY
Winding 1 Line-to-Line Voltage (1.00–1000.00 kV)	VWDG 1	=	66
Winding 2 Line-to-Line Voltage (1.00–1000.00 kV)	VWDG 2	=	11

Differential Elements
Note: TAP1 and TAP2 are auto-set by relay if MVA setting is not OFF.

Winding 1 Current Tap			
(0.50–155.00 A secondary) (5 A)			
(0.10–31.00 A secondary) (1 A)	TAP1	=	5.25
Winding 2 Current Tap			
(0.50–155.00 A secondary) (5 A)			
(0.10–31.00 A secondary) (1 A)	TAP2	=	5.25
Restrained Element Operating Current PU (0.10–1.00 TAP)	O87P	=	0.30

Restraint Slope 1 Percentage (5–100%)	SLP1	=	25
Restraint Slope 2 Percentage (OFF, 25–200%)	SLP2	=	50
Restraint Current Slope 1 Limit (1.0–20.0 TAP)	IRS1	=	3.0
Unrestrained Element Current PU (1–20 TAP)	U87P	=	10.0
Second-Harmonic Blocking Percentage (OFF, 5–100%)	PCT2	=	15
Fourth-Harmonic Blocking Percentage (OFF, 5–100%)	PCT4	=	15
Fifth-Harmonic Blocking Percentage (OFF, 5–100%)	PCT5	=	35
Fifth-Harmonic Alarm Threshold (OFF, 0.02–3.2 TAP)	TH5P	=	OFF
Fifth-Harmonic Alarm TDPU (0.000–8000.000 cyc)	TH5D	=	
DC Ratio Blocking (Y, N)	DCRB	=	N
Harmonic Restraint (Y, N)	HRSTR	=	N
Independent Harmonic Blocking (Y, N)	IHBL	=	N

Restricted Earth Fault
Enable 32I (SELogic control equation)
E32I1 = 0

Operating Quantity from Wdg. 1, Wdg. 2 (1, 2, 12)	32IOP1	=	
Positive-Sequence Current Restraint Factor, I0/I1 (0.02–0.50)	a01	=	
Residual Current Sensitivity Threshold (0.25–15 A secondary) (5 A) (0.05–3 A secondary) (1 A)	50GP1	=	

Enable 32I (SELogic control equation)
E32I2 = 0

Operating Quantity from Wdg. 1, Wdg. 2 (1, 2, 12)	32IOP2	=	
Positive-Sequence Current Restraint Factor, I0/I1 (0.02–0.50)	a02	=	
Residual Current Sensitivity Threshold (0.25–15 A secondary) (5 A) (0.05–3 A secondary) (1 A)	50GP2	=	

Winding 1 O/C Elements

Winding 1 Phase O/C Elements

Phase Def.-Time O/C Level 1 PU (OFF, 0.25–100 A secondary) (5 A) (OFF, 0.05–20 A secondary) (1 A)	50P11P	=	
Phase Level 1 O/C Delay (0.00–16000.00 cycles)	50P11D	=	

50P11 Torque Control (SELogic control equation)
50P11TC =

Phase Inst. O/C Level 2 PU (OFF, 0.25–100 A secondary) (5 A) (OFF, 0.05–20 A secondary) (1 A)	50P12P	=	

50P12 Torque Control (SELogic control equation)
50P12TC =

Phase Inst. O/C Level 3 PU (OFF, 0.25–100 A secondary) (5 A) (OFF, 0.05–20 A secondary) (1 A)	50P13P	=	

Phase Inst. O/C Level 4 PU

(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50P14P = ________
Phase Inv.-Time O/C PU
(OFF, 0.50–16.00 A secondary) (5 A)
(OFF, 0.10–3.20 A secondary) (1 A) 51P1P = ________
Phase Inv.-Time O/C Curve (U1–U5, C1–C5) 51P1C = ________
Phase Inv.-Time O/C Time-Dial (US 0.5–15.0, IEC 0.05–1.00) 51P1TD = ________
Phase Inv.-Time O/C EM Reset (Y, N) 51P1RS = ________
51P1 Torque Control (SELogic control equation)
51P1TC = ____

Winding 1 Negative-Sequence O/C Elements
Note: All negative-sequence element pickup settings are in terms of 3I2.
Neg.-Seq. Def.-Time O/C Level 1 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50Q11P = ________
Neg.-Seq. Level 1 O/C Delay (0.50–16000.00 cycles) 50Q11D = ________
50Q11 Torque Control (SELogic control equation)
50Q11TC = ____
Neg.-Seq. Inst. O/C Level 2 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50Q12P = ________
50Q12 Torque Control (SELogic control equation)
50Q12TC = ____
Neg.-Seq. Inv.-Time O/C PU
(OFF, 0.50–16.00 A secondary) (5 A)
(OFF, 0.10–3.20 A secondary) (1 A) 51Q1P = ________
Neg.-Seq. Inv.-Time O/C Curve (U1–U5, C1–C5) 51Q1C = ________
Neg.-Seq. Inv.-Time O/C Time-Dial (US 0.5–15, IEC 0.05–1.00) 51Q1TD = ________
Neg.-Seq. Inv.-Time O/C EM Reset (Y, N) 51Q1RS = ________
51Q1 Torque Control (SELogic control equation)
51Q1TC = ____

Winding 1 Residual O/C Elements
Residual Def.-Time O/C Level 1 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50N11P = ________
Residual Level 1 O/C Delay (0.00–16000.00 cycles) 50N11D = ________
50N11 Torque Control (SELogic control equation)
50N11TC = ____
Residual Inst. O/C Level 2 PU
(OFF, 0.25–100.00 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50N12P = ________
50N12 Torque Control (SELogic control equation)
50N12TC = ____
Residual Inv.-Time O/C PU
(OFF, 0.50–16.00 A secondary) (5 A)

(OFF, 0.10–3.20 A secondary) (1 A) 51N1P = ________
Residual Inv.-Time O/C Curve (U1–U5, C1–C5) 51N1C = ________
Residual Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00) 51N1TD = ________
Residual Inv.-Time O/C EM Reset (Y, N) 51N1RS = ________
51N1 Torque Control (SELogic control equation)
51N1TC = ____

Winding 1 Demand Metering
Demand Ammeter Time Constant (OFF, 5–255 min) DATC1 = ________
Phase Demand Ammeter Threshold
(0.50–16.00 A secondary) (5 A)
(0.10–3.20 A secondary) (1 A) PDEM1P = ________
Neg.-Seq. Demand Ammeter Threshold
(0.50–16.00 A secondary) (5 A)
(0.10–3.20 A secondary) (1 A) QDEM1P = ________
Residual Demand Ammeter Threshold
(0.50–16.00 A secondary) (5 A)
(0.10–3.20 A secondary) (1 A) NDEM1P = ________

Winding 2 O/C Elements

Winding 2 Phase O/C Elements
Phase Def.-Time O/C Level 1 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50P21P = ________
Phase Level 1 O/C Delay (0.00–16000.00 cycles) 50P21D = ________
50P21 Torque Control (SELogic control equation)
50P21TC = ____
Phase Inst. O/C Level 2 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50P22P = ________
50P22 Torque Control (SELogic control equation)
50P22TC = ____
Phase Inst. O/C Level 3 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50P23P = ________
Phase Inst. O/C Level 4 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50P24P = ________
Phase Inv.-Time O/C PU
(OFF, 0.50–16.00 A secondary) (5 A)
(OFF, 0.10–3.20 A secondary) (1 A) 51P2P = ________
Phase Inv.-Time O/C Curve (U1–U5, C1–C5) 51P2C = ________
Phase Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00) 51P2TD = ________

Phase Inv.-Time O/C EM Reset (Y, N) 51P2RS = __________
51P2 Torque Control (SELogic control equation)
51P2TC = ____

Winding 2 Negative-Sequence O/C Elements
Note: All negative-sequence element pickup settings are in terms of 3I2.
Neg.-Seq. Def.-Time O/C Level 1 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50Q21P = __________
Neg.-Seq. Level 1 O/C Delay (0.50–16000.00 cycles) 50Q21D = __________
50Q21 Torque Control (SELogic control equation)
50Q21TC = ____
Neg.-Seq. Inst. O/C Level 2 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50Q22P = __________
50Q22 Torque Control (SELogic control equation)
50Q22TC = ____
Neg.-Seq. Inv.-Time O/C PU
(OFF, 0.50–16.00 A secondary) (5 A)
(OFF, 0.10–3.20 A secondary) (1 A) 51Q2P = __________
Neg.-Seq. Inv.-Time O/C Curve (U1–U5, C1–C5) 51Q2C = __________
Neg.-Seq. Inv.-Time O/C Time-Dial (US 0.5–15, IEC 0.05–1.00) 51Q2TD = __________
Neg.-Seq. Inv.-Time O/C EM Reset (Y, N) 51Q2RS = __________
51Q2 Torque Control (SELogic control equation)
51Q2TC = ____

Winding 2 Residual O/C Elements
Residual Def.-Time O/C Level 1 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50N21P = __________
Residual Level 1 O/C Delay (0.00–16000.00 cycles) 50N21D = __________
50N21 Torque Control (SELogic control equation)
50N21TC = ____
Residual Inst. O/C Level 2 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50N22P = __________
50N22 Torque Control (SELogic control equation)
50N22TC = ____
Residual Inv.-Time O/C PU
(OFF, 0.50–16.00 A secondary) (5 A)
(OFF, 0.10–3.20 A secondary) (1 A) 51N2P = __________
Residual Inv.-Time O/C Curve (U1–U5, C1–C5) 51N2C = __________
Residual Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00) 51N2TD = __________
Residual Inv.-Time O/C EM Reset (Y, N) 51N2RS = __________
51N2 Torque Control (SELogic control equation)
51N2TC = ____

Winding 2 Demand Metering		
Demand Ammeter Time Constant (OFF, 5–255 min)	DATC2	= ______
Phase Demand Ammeter Threshold (0.05–16.00 A secondary) (5 A) (0.10–3.20 A secondary) (1 A)	PDEM2P	= ______
Neg.-Seq. Demand Ammeter Threshold (0.50–16.00 A secondary) (5 A) (0.10–3.20 A secondary) (1 A)	QDEM2P	= ______
Residual Demand Ammeter Threshold (0.50–16.00 A secondary) (5 A) (0.10–3.20 A secondary) (1 A)	NDEM2P	= ______

Neutral Elements

Neutral 1 Elements		
Neutral Def.-Time O/C Level 1 PU (OFF, 0.25–100 A secondary) (5 A) (OFF, 0.05–20 A secondary) (1 A)	50NN11P	= ______
Neutral Level 1 O/C Delay (0.00–16000.00 cycles)	50NN11D	= ______

50NN11 Torque Control (SELogic control equation)
50NN11TC = ______________________________

Neutral Inst. O/C Level 2 PU (OFF, 0.25–100 A secondary) (5 A) (OFF, 0.05–20 A secondary) (1 A)	50NN12P	= ______

50NN12 Torque Control (SELogic control equation)
50NN12TC = ______________________________

Neutral Inst. O/C Level 3 PU (OFF, 0.25–100 A secondary) (5 A) (OFF, 0.05–20 A secondary) (1 A)	50NN13P	= ______
Neutral Inst. O/C Level 4 PU (OFF, 0.25–100 A secondary) (5 A) (OFF, 0.05–20 A secondary) (1 A)	50NN14P	= ______
Neutral Inv.-Time O/C PU (OFF, 0.50–16.00 A secondary) (5 A) (OFF, 0.10–3.20 A secondary) (1 A)	51NN1P	= ______
Neutral Inv.-Time O/C Curve (U1–U5, C1–C5)	51NN1C	= ______
Neutral Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00)	51NN1TD	= ______
Neutral Inv.-Time O/C EM Reset (Y, N)	51NN1R	= ______

S ______

51NN1 Torque Control (SELogic control equation)
51NN1TC = ____________________

Neutral 2 Elements
Neutral Def.-Time O/C Level 1 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50NN21P = ______
Neutral Level 1 O/C Delay (0.00–16000.00 cycles) 50NN21D = ______
50NN21 Torque Control (SELogic control equation)
50NN21TC = ____________________
Neutral Inst. O/C Level 2 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50NN22P = ______
50NN22 Torque Control (SELogic control equation)
50NN22TC = ____________________
Neutral Inst. O/C Level 3 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50NN23P = ______
Neutral Inst. O/C Level 4 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50NN24P = ______
Neutral Inv.-Time O/C PU
(OFF, 0.50–16.00 A secondary) (5 A)
(OFF, 0.10–3.20 A secondary) (1 A) 51NN2P = ______
Neutral Inv.-Time O/C Curve (U1–U5, C1–C5) 51NN2C = ______
Neutral Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00) 51NN2TD = ______
Neutral Inv.-Time O/C EM Reset (Y, N) 51NN2RS = ______
51NN2 Torque Control (SELogic control equation)
51NN2TC = ____________________

Neutral 3 Elements
Neutral Def.-Time O/C Level 1 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50NN31P = ______
Neutral Level 1 O/C Delay (0.00–16000.00 cycles) 50NN31D = ______
50NN31 Torque Control (SELogic control equation)
50NN31TC = ____________________

Neutral Inst. O/C Level 2 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50NN32P = __________

50NN32 Torque Control (SELogic control equation)
50NN32TC = ____

Neutral Inst. O/C Level 3 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50NN33P = __________

Neutral Inst. O/C Level 4 PU
(OFF, 0.25–100 A secondary) (5 A)
(OFF, 0.05–20 A secondary) (1 A) 50NN34P = __________

Neutral Inv.-Time O/C PU
(OFF, 0.50–16.00 A secondary) (5 A)
(OFF, 0.10–3.20 A secondary) (1 A) 51NN3P = __________

Neutral Inv.-Time O/C Curve (U1–U5, C1–C5) 51NN3C = __________

Neutral Inv.-Time O/C Time-Dial (US 0.50–15.00, IEC 0.05–1.00) 51NN3TD = __________

Neutral Inv.-Time O/C EM Reset (Y, N) 51NN3RS = __________

51NN3 Torque Control (SELogic control equation)
51NN3TC = ____

RTD A Elements

RTD 1A Alarm Temperature (OFF, 32–482°F)	49A01A	=__________
RTD 1A Trip Temperature (OFF, 32–482°F)	49T01A	=__________
RTD 2A Alarm Temperature (OFF, 32–482°F)	49A02A	=__________
RTD 2A Trip Temperature (OFF, 32–482°F)	49T02A	=__________
RTD 3A Alarm Temperature (OFF, 32–482°F)	49A03A	=__________
RTD 3A Trip Temperature (OFF, 32–482°F)	49T03A	=__________
RTD 4A Alarm Temperature (OFF, 32–482°F)	49A04A	=__________
RTD 4A Trip Temperature (OFF, 32–482°F)	49T04A	=__________
RTD 5A Alarm Temperature (OFF, 32–482°F)	49A05A	=__________
RTD 5A Trip Temperature (OFF, 32–482°F)	49T05A	=__________
RTD 6A Alarm Temperature (OFF, 32–482°F)	49A06A	=__________
RTD 6A Trip Temperature (OFF, 32–482°F)	49T06A	=__________
RTD 7A Alarm Temperature (OFF, 32–482°F)	49A07A	=__________
RTD 7A Trip Temperature (OFF, 32–482°F)	49T07A	=__________
RTD 8A Alarm Temperature (OFF, 32–482°F)	49A08A	=__________
RTD 8A Trip Temperature (OFF, 32–482°F)	49T08A	=__________
RTD 9A Alarm Temperature (OFF, 32–482°F)	49A09A	=__________
RTD 9A Trip Temperature (OFF, 32–482°F)	49T09A	=__________
RTD 10A Alarm Temperature (OFF, 32–482°F)	49A10A	=__________
RTD 10A Trip Temperature (OFF, 32–482°F)	49T10A	=__________
RTD 11A Alarm Temperature (OFF, 32–482°F)	49A11A	=__________

RTD 11A Trip Temperature (OFF, 32–482°F)	49T11A	= ________
RTD 12A Alarm Temperature (OFF, 32–482°F)	49A12A	= ________
RTD 12A Trip Temperature (OFF, 32–482°F)	49T12A	= ________

RTD B Elements

RTD 1B Alarm Temperature (OFF, 32–482°F)	49A01B	= ________
RTD 1B Trip Temperature (OFF, 32–482°F)	49T01B	= ________
RTD 2B Alarm Temperature (OFF, 32–482°F)	49A02B	= ________
RTD 2B Trip Temperature (OFF, 32–482°F)	49T02B	= ________
RTD 3B Alarm Temperature (OFF, 32–482°F)	49A03B	= ________
RTD 3B Trip Temperature (OFF, 32–482°F)	49T03B	= ________
RTD 4B Alarm Temperature (OFF, 32–482°F)	49A04B	= ________
RTD 4B Trip Temperature (OFF, 32–482°F)	49T04B	= ________
RTD 5B Alarm Temperature (OFF, 32–482°F)	49A05B	= ________
RTD 5B Trip Temperature (OFF, 32–482°F)	49T05B	= ________
RTD 6B Alarm Temperature (OFF, 32–482°F)	49A06B	= ________
RTD 6B Trip Temperature (OFF, 32–482°F)	49T06B	= ________
RTD 7B Alarm Temperature (OFF, 32–482°F)	49A07B	= ________
RTD 7B Trip Temperature (OFF, 32–482°F)	49T07B	= ________
RTD 8B Alarm Temperature (OFF, 32–482°F)	49A08B	= ________
RTD 8B Trip Temperature (OFF, 32–482°F)	49T08B	= ________
RTD 9B Alarm Temperature (OFF, 32–482°F)	49A09B	= ________
RTD 9B Trip Temperature (OFF, 32–482°F)	49T09B	= ________
RTD 10B Alarm Temperature (OFF, 32–482°F)	49A10B	= ________
RTD 10B Trip Temperature (OFF, 32–482°F)	49T10B	= ________
RTD 11B Alarm Temperature (OFF, 32–482°F)	49A11B	= ________
RTD 11B Trip Temperature (OFF, 32–482°F)	49T11B	= ________
RTD 12B Alarm Temperature (OFF, 32–482°F)	49A12B	= ________
RTD 12B Trip Temperature (OFF, 32–482°F)	49T12B	= ________

Miscellaneous Timers

Minimum Trip Duration Time Delay (4.000–8000.000 cycles)	TDURD	= 9.0
Close Failure Logic Time Delay (OFF, 0.000–8000.000 cycles)	CFD	= 60.0

SELogic Control Equations Set 1

Set 1 Variable 1 (SELogic control equation)

S1V1 = ____

S1V1 Timer Pickup (OFF, 0.000–999999.000 cycles)	S1V1PU	= ________
S1V1 Timer Dropout (OFF, 0.000–999999.000 cycles)	S1V1DO	= ________

Set 1 Variable 2 (SELogic control equation)

S1V2 = ____

S1V2 Timer Pickup (OFF, 0.000–999999.000 cycles)	S1V2PU	= ________
S1V2 Timer Dropout (OFF, 0.000–999999.000 cycles)	S1V2DO	= ________

Set 1 Variable 3 (SELogic control equation)

S1V3 = ____

S1V3 Timer Pickup (OFF, 0.000–999999.000 cycles)	S1V3PU	= ________

S1V3 Timer Dropout (OFF, 0.000–999999.000 cycles) S1V3DO = __________
Set 1 Variable 4 (SELogic control equation)
S1V4 = ________________________________
S1V4 Timer Pickup (OFF, 0.000–999999.000 cycles) S1V4PU = __________
S1V4 Timer Dropout (OFF, 0.000–999999.000 cycles) S1V4DO = __________
Set 1 Latch Bit 1 SET Input (SELogic control equation)
S1SLT1 = ________________________________
Set 1 Latch Bit 1 RESET Input (SELogic control equation)
S1RLT1 = ________________________________
Set 1 Latch Bit 2 SET Input (SELogic control equation)
S1SLT2 = ________________________________
Set 1 Latch Bit 2 RESET Input (SELogic control equation)
S1RLT2 = ________________________________
Set 1 Latch Bit 3 SET Input (SELogic control equation)
S1SLT3 = ________________________________
Set 1 Latch Bit 3 RESET Input (SELogic control equation)
S1RLT3 = ________________________________
Set 1 Latch Bit 4 SET Input (SELogic control equation)
S1SLT4 = ________________________________
Set 1 Latch Bit 4 RESET Input (SELogic control equation)
S1RLT4 = ________________________________

SELogic Control Equations Set 2
Set 2 Variable 1 (SELogic control equation)
S2V1 = ________________________________
S2V1 Timer Pickup (OFF, 0.000–999999.000 cycles) S2V1PU = __________
S2V1 Timer Dropout (OFF, 0.000–999999.000 cycles) S2V1DO = __________
Set 2 Variable 2 (SELogic control equation)
S2V2 = ________________________________
S2V2 Timer Pickup (OFF, 0.000–999999.000 cycles) S2V2PU = __________
S2V2 Timer Dropout (OFF, 0.000–999999.000 cycles) S2V2DO = __________
Set 2 Variable 3 (SELogic control equation)
S2V3 = ________________________________
S2V3 Timer Pickup (OFF, 0.000–999999.000 cycles) S2V3PU = __________
S2V3 Timer Dropout (OFF, 0.000–999999.000 cycles) S2V3DO = __________
Set 2 Variable 4 (SELogic control equation)
S2V4 = ________________________________
S2V4 Timer Pickup (OFF, 0.000–999999.000 cycles) S2V4PU = __________
S2V4 Timer Dropout (OFF, 0.000–999999.000 cycles) S2V4DO = __________
Set 2 Latch Bit 1 SET Input (SELogic control equation)
S2SLT1 = ________________________________
Set 2 Latch Bit 1 RESET Input (SELogic control equation)

S2RLT1 = ____
Set 2 Latch Bit 2 SET Input (SELogic control equation)
S2SLT2 = ____
Set 2 Latch Bit 2 RESET Input (SELogic control equation)
S2RLT2 = ____
Set 2 Latch Bit 3 SET Input (SELogic control equation)
S2SLT3 = ____
Set 2 Latch Bit 3 RESET Input (SELogic control equation)
S2RLT3 = ____
Set 2 Latch Bit 4 SET Input (SELogic control equation)
S2SLT4 = ____
Set 2 Latch Bit 4 RESET Input (SELogic control equation)
S2RLT4 = ____

SELogic Control Equations Set 3
Set 3 Variable 1 (SELogic control equation)
S3V1 = ____
S3V1 Timer Pickup (OFF, 0.000–999999.000 cycles) S3V1PU =__________
S3V1 Timer Dropout (OFF, 0.000–999999.000 cycles) S3V1DO =__________
Set 3 Variable 2 (SELogic control equation)
S3V2 = ____
S3V2 Timer Pickup (OFF, 0.000–999999.000 cycles) S3V2PU =__________
S3V2 Timer Dropout (OFF, 0.000–999999.000 cycles) S3V2DO =__________
Set 3 Variable 3 (SELogic control equation)
S3V3 = ____
S3V3 Timer Pickup (OFF, 0.000–999999.000 cycles) S3V3PU =__________
S3V3 Timer Dropout (OFF, 0.000–999999.000 cycles) S3V3DO =__________
Set 3 Variable 4 (SELogic control equation)
S3V4 = ____
S3V4 Timer Pickup (OFF, 0.000–999999.000 cycles) S3V4PU =__________
S3V4 Timer Dropout (OFF, 0.000–999999.000 cycles) S3V4DO =__________
Set 3 Variable 5 (SELogic control equation)
S3V5 = ____
S3V5 Timer Pickup (OFF, 0.000–999999.000 cycles) S3V5PU =__________
S3V5 Timer Dropout (OFF, 0.000–999999.000 cycles) S3V5DO =__________
Set 3 Variable 6 (SELogic control equation)
S3V6 = ____
S3V6 Timer Pickup (OFF, 0.000–999999.000 cycles) S3V6PU =__________
S3V6 Timer Dropout (OFF, 0.000–999999.000 cycles) S3V6DO =__________
Set 3 Variable 7 (SELogic control equation)
S3V7 = ____
S3V7 Timer Pickup (OFF, 0.000–999999.000 cycles) S3V7PU =__________
S3V7 Timer Dropout (OFF, 0.000–999999.000 cycles) S3V7DO =__________
Set 3 Variable 8 (SELogic control equation)
S3V8 = ____
S3V8 Timer Pickup (OFF, 0.000–999999.000 cycles) S3V8PU =__________
S3V8 Timer Dropout (OFF, 0.000–999999.000 cycles) S3V8DO =__________

Set 3 Latch Bit 1 SET Input (SELogic control equation)
S3SLT1 = ____________________
Set 3 Latch Bit 1 RESET Input (SELogic control equation)
S3RLT1 = ____________________
Set 3 Latch Bit 2 SET Input (SELogic control equation)
S3SLT2 = ____________________
Set 3 Latch Bit 2 RESET Input (SELogic control equation)
S3RLT2 = ____________________
Set 3 Latch Bit 3 SET Input (SELogic control equation)
S3SLT3 = ____________________
Set 3 Latch Bit 3 RESET Input (SELogic control equation)
S3RLT3 = ____________________
Set 3 Latch Bit 4 SET Input (SELogic control equation)
S3SLT4 = ____________________
Set 3 Latch Bit 4 RESET Input (SELogic control equation)
S3RLT4 = ____________________
Set 3 Latch Bit 5 SET Input (SELogic control equation)
S3SLT5 = ____________________
Set 3 Latch Bit 5 RESET Input (SELogic control equation)
S3RLT5 = ____________________
Set 3 Latch Bit 6 SET Input (SELogic control equation)
S3SLT6 = ____________________
Set 3 Latch Bit 6 RESET Input (SELogic control equation)
S3RLT6 = ____________________
Set 3 Latch Bit 7 SET Input (SELogic control equation)
S3SLT7 = ____________________
Set 3 Latch Bit 7 RESET Input (SELogic control equation)
S3RLT7 = ____________________
Set 3 Latch Bit 8 SET Input (SELogic control equation)
S3SLT8 = ____________________
Set 3 Latch Bit 8 RESET Input (SELogic control equation)
S3RLT8 = ____________________

Trip Logic

TR1	=	50P11T+51P1T+51Q1T+OC1+LB3+87R+87U+51P2T+51Q2T+OC2
TR2	=	50P11T+51P1T+51Q1T+OC1+LB3+87R+87U+51P2T+51Q2T+OC2
TR3	=	50P11T+51P1T+51Q1T+OC1+LB3+87R+87U+51P2T+51Q2T+OC2
TR4	=	0
TR5	=	0
ULTR1	=	!50P13
ULTR2	=	!50P23
ULTR3	=	!(50P13+50P23)
ULTR4	=	0
ULTR5	=	0

Close Logic

52A1 = IN101

52A2	=	IN102
52A3	=	0
52A4	=	0
CL1	=	CC1+LB4+/IN104
CL2	=	CC2+/IN105
CL3	=	0
CL4	=	0
ULCL1	=	TRIP1+TRIP3
ULCL2	=	TRIP2+TRIP3
ULCL3	=	0
ULCL4	=	0

Event Report Triggering

ER	=	/50P11+/51P1+/51Q1+/51P2+/51Q2

Output Contact Logic (Standard Outputs)

OUT101	=	TRIP1
OUT102	=	TRIP2
OUT103	=	TRIP3
OUT104	=	0
OUT105	=	CLS1
OUT106	=	CLS2
OUT107	=	0

Output Contact Logic (Extra Interface Board 2 or 6)

OUT201	=	
OUT202	=	
OUT203	=	
OUT204	=	
OUT205	=	
OUT206	=	
OUT207	=	
OUT208	=	
OUT209	=	
OUT210	=	
OUT211	=	
OUT212	=	

Output Contact Logic (Extra Interface Board 4)

OUT201	=	
OUT202	=	
OUT203	=	
OUT204	=	

Relay Settings

Length of Event Report (15, 30, 60 cycles) LER = 15

Length of Pre-fault in Event Report (1 to 14 cycles)	PRE	=	14
Nominal Frequency (50, 60 Hz)	NFREQ	=	50
Phase Rotation (ABC, ACB)	PHROT	=	ABC
Date Format (MDY, YMD)	DATE_F	=	MDY
Display Update Rate (1–60 seconds)	SCROLD	=	1
Front Panel Time-out (OFF, 0–30 minutes)	FP_TO	=	15
Group Change Delay (0–900 seconds)	TGR	=	3
RTDA Temperature Preference (C, F)	TMPREF A	=	C
RTDB Temperature Preference (C, F)	TMPREF B	=	C

Battery Monitor

DC Battery Voltage Level 1 (OFF, 20–300 Vdc)	DC1P	=	OFF
DC Battery Voltage Level 2 (OFF, 20–300 Vdc)	DC2P	=	OFF
DC Battery Voltage Level 3 (OFF, 20–300 Vdc)	DC3P	=	OFF
DC Battery Voltage Level 4 (OFF, 20–300 Vdc)	DC4P	=	OFF

Debounce Timers

Input debounce time (0.00–2.00 cyc)	IN101D	=	0.13
Input debounce time (0.00–2.00 cyc)	IN102D	=	0.13
Input debounce time (0.00–2.00 cyc)	IN103D	=	0.13
Input debounce time (0.00–2.00 cyc)	IN104D	=	0.13
Input debounce time (0.00–2.00 cyc)	IN105D	=	0.13
Input debounce time (0.00–2.00 cyc)	IN106D	=	0.13
Input debounce time (0.00–2.00 cyc)	IN201D	=	
Input debounce time (0.00–2.00 cyc)	IN202D	=	
Input debounce time (0.00–2.00 cyc)	IN203D	=	
Input debounce time (0.00–2.00 cyc)	IN204D	=	
Input debounce time (0.00–2.00 cyc)	IN205D	=	
Input debounce time (0.00–2.00 cyc)	IN206D	=	
Input debounce time (0.00–2.00 cyc)	IN207D	=	
Input debounce time (0.00–2.00 cyc)	IN208D	=	

Breaker 1 Monitor
BKR1 Trigger Equation (SELogic control equation)
BKMON1 = TRIP1+TRIP3

Close/Open Set Point 1 max (1–65000 operations)	B1COP1	=	10000
kA Interrupted Set Point 1 min (0.1–999.0 kA pri)	B1KAP1	=	1.2
Close/Open Set Point 2 max (1–65000 operations)	B1COP2	=	150
kA Interrupted Set Point 2 min (0.1–999.0 kA pri)	B1KAP2	=	8.0
Close/Open Set Point 3 max (1–65000 operations)	B1COP3	=	12
kA Interrupted Set Point 3 min (0.1–999.0 kA pri)	B1KAP3	=	20.0

Breaker 2 Monitor
BKR2 Trigger Equation (SELogic control equation)
BKMON2 = TRIP2+TRIP3

Close/Open Set Point 1 max (1–65000 operations)	B2COP1	=	10000

kA Interrupted Set Point 1 min (0.1–999.0 kA pri)	B2KAP1	= 1.2
Close/Open Set Point 2 max (1–65000 operations)	B2COP2	= 150
kA Interrupted Set Point 2 min (0.1–999.0 kA pri)	B2KAP2	= 8.0
Close/Open Set Point 3 max (1–65000 operations)	B2COP3	= 12
kA Interrupted Set Point 3 min (0.1–999.0 kA pri)	B2KAP3	= 20.0

Analog Input Labels

Rename Current Input IAW1 (1–4 characters)	IAW1	= IAW1
Rename Current Input IBW1 (1–4 characters)	IBW1	= IBW1
Rename Current Input ICW1 (1–4 characters)	ICW1	= ICW1
Rename Current Input IAW2 (1–4 characters)	IAW2	= IAW2
Rename Current Input IBW2 (1–4 characters)	IBW2	= IBW2
Rename Current Input ICW2 (1–4 characters)	ICW2	= ICW2
Rename Current Input IAW4 (1–4 characters)	IAW4 (IN1)	= IN1
Rename Current Input IBW4 (1–4 characters)	IBW4 (IN2)	= IN2
Rename Current Input ICW4 (1–4 characters)	ICW4 (IN3)	= IN3

Setting Group Selection

Select Setting Group 1 (SELogic control equation)
SS1 = 0

Select Setting Group 2 (SELogic control equation)
SS2 = 0

Select Setting Group 3 (SELogic control equation)
SS3 = 0

Select Setting Group 4 (SELogic control equation)
SS4 = 0

Select Setting Group 5 (SELogic control equation)
SS5 = 0

Select Setting Group 6 (SELogic control equation)
SS6 = 0

Front Panel

Energize LEDA (SELogic control equation)
LEDA = OCA+87E1

Energize LEDB (SELogic control equation)
LEDB = OCB+87E2

Energize LEDC (SELogic control equation)
LEDC = OCC+87E3

Show Display Point 1 (SELogic control equation)
DP1 = IN101

DP1 Label 1 (16 characters) (Enter NA to Null)	DP1_1	= BREAKER 1 CLOSED
DP1 Label 0 (16 characters) (Enter NA to Null)	DP1_0	= BREAKER 1 OPEN

Show Display Point 2 (SELogic control equation)

DP2 = IN102

DP2 Label 1 (16 characters) (Enter NA to Null)	DP2_1	=	BREAKER 2 CLOSED
DP2 Label 0 (16 characters) (Enter NA to Null)	DP2_0	=	BREAKER 2 OPEN

Show Display Point 3 (SELogic control equation)
DP3 = 0

DP3 Label 1 (16 characters) (Enter NA to Null)	DP3_1	=	
DP3 Label 0 (16 characters) (Enter NA to Null)	DP3_0	=	

Show Display Point 4 (SELogic control equation)
DP4 = 0

DP4 Label 1 (16 characters) (Enter NA to Null)	DP4_1	=	
DP4 Label 0 (16 characters) (Enter NA to Null)	DP4_0	=	

Show Display Point 5 (SELogic control equation)
DP5 = 0

DP5 Label 1 (16 characters) (Enter NA to Null)	DP5_1	=	
DP5 Label 0 (16 characters) (Enter NA to Null)	DP5_0	=	

Show Display Point 6 (SELogic control equation)
DP6 = 0

DP6 Label 1 (16 characters) (Enter NA to Null)	DP6_1	=	
DP6 Label 0 (16 characters) (Enter NA to Null)	DP6_0	=	

Show Display Point 7 (SELogic control equation)
DP7 = 0

DP7 Label 1 (16 characters) (Enter NA to Null)	DP7_1	=	
DP7 Label 0 (16 characters) (Enter NA to Null)	DP7_0	=	

Show Display Point 8 (SELogic control equation)
DP8 = 0

DP8 Label 1 (16 characters) (Enter NA to Null)	DP8_1	=	
DP8 Label 0 (16 characters) (Enter NA to Null)	DP8_0	=	

Show Display Point 9 (SELogic control equation)
DP9 = 0

DP9 Label 1 (16 characters) (Enter NA to Null)	DP9_1	=	
DP9 Label 0 (16 characters) (Enter NA to Null)	DP9_0	=	

Show Display Point 10 (SELogic control equation)
DP10 = 0

DP10 Label 1 (16 characters) (Enter NA to Null)	DP10_1	=	
DP10 Label 0 (16 characters) (Enter NA to Null)	DP10_0	=	

Show Display Point 11 (SELogic control equation)
DP11 = 0

DP11 Label 1 (16 characters) (Enter NA to Null)	DP11_1	=	
DP11 Label 0 (16 characters) (Enter NA to Null)	DP11_0	=	

Show Display Point 12 (SELogic control equation)
DP12 = 0

DP12 Label 1 (16 characters) (Enter NA to Null)	DP12_1	=	
DP12 Label 0 (16 characters) (Enter NA to Null)	DP12_0	=	

Show Display Point 13 (SELogic control equation)
DP13 = 0

DP13 Label 1 (16 characters) (Enter NA to Null)	DP13_1	=	
DP13 Label 0 (16 characters) (Enter NA to Null)	DP13_0	=	

Show Display Point 14 (SELogic control equation)
DP14 = 0

DP14 Label 1 (16 characters) (Enter NA to Null)	DP14_1	=	
DP14 Label 0 (16 characters) (Enter NA to Null)	DP14_0	=	

Energize LED15 (SELogic control equation)
DP15 = 0

Energize LED16 (SELogic control equation)
DP16 = 0

Text Labels

Local Bit LB1 Name (14 characters) (Enter NA to Null)	NLB1	=	
Clear Local Bit LB1 Label (7 characters) (Enter NA to Null)	CLB1	=	
Set Local Bit LB1 Label (7 characters) (Enter NA to Null)	SLB1	=	
Pulse Local Bit LB1 Label (7 characters) (Enter NA to Null)	PLB1	=	
Local Bit LB2 Name (14 characters) (Enter NA to Null)	NLB2	=	
Clear Local Bit LB2 Label (7 characters) (Enter NA to Null)	CLB2	=	
Set Local Bit LB2 Label (7 characters) (Enter NA to Null)	SLB2	=	
Pulse Local Bit LB2 Label (7 characters) (Enter NA to Null)	PLB2	=	
Local Bit LB3 Name (14 characters) (Enter NA to Null)	NLB3	=	MANUAL TRIP 1
Clear Local Bit LB3 Label (7 characters) (Enter NA to Null)	CLB3	=	RETURN
Set Local Bit LB3 Label (7 characters) (Enter NA to Null)	SLB3	=	
Pulse Local Bit LB3 Label (7 characters) (Enter NA to Null)	PLB3	=	TRIP
Local Bit LB4 Name (14 characters) (Enter NA to Null)	NLB4	=	MANUAL CLOSE
Clear Local Bit LB4 Label (7 characters) (Enter NA to Null)	CLB4	=	RETURN
Set Local Bit LB4 Label (7 characters) (Enter NA to Null)	SLB4	=	
Pulse Local Bit LB4 Label (7 characters) (Enter NA to Null)	PLB4	=	CLOSE
Local Bit LB5 Name (14 characters) (Enter NA to Null)	NLB5	=	
Clear Local Bit LB5 Label (7 characters) (Enter NA to Null)	CLB5	=	
Set Local Bit LB5 Label (7 characters) (Enter NA to Null)	SLB5	=	
Pulse Local Bit LB5 Label (7 characters) (Enter NA to Null)	PLB5	=	
Local Bit LB6 Name (14 characters) (Enter NA to Null)	NLB6	=	
Clear Local Bit LB6 Label (7 characters) (Enter NA to Null)	CLB6	=	
Set Local Bit LB6 Label (7 characters) (Enter NA to Null)	SLB6	=	

Pulse Local Bit LB6 Label (7 characters) (Enter NA to Null)	PLB6	=	______
Local Bit LB7 Name (14 characters) (Enter NA to Null)	NLB7	=	______
Clear Local Bit LB7 Label (7 characters) (Enter NA to Null)	CLB7	=	______
Set Local Bit LB7 Label (7 characters) (Enter NA to Null)	SLB7	=	______
Pulse Local Bit LB7 Label (7 characters) (Enter NA to Null)	PLB7	=	______
Local Bit LB8 Name (14 characters) (Enter NA to Null)	NLB8	=	______
Clear Local Bit LB8 Label (7 characters) (Enter NA to Null)	CLB8	=	______
Set Local Bit LB8 Label (7 characters) (Enter NA to Null)	SLB8	=	______
Pulse Local Bit LB8 Label (7 characters) (Enter NA to Null)	PLB8	=	______
Local Bit LB9 Name (14 characters) (Enter NA to Null)	NLB9	=	______
Clear Local Bit LB9 Label (7 characters) (Enter NA to Null)	CLB9	=	______
Set Local Bit LB9 Label (7 characters) (Enter NA to Null)	SLB9	=	______
Pulse Local Bit LB9 Label (7 characters) (Enter NA to Null)	PLB9	=	______
Local Bit LB10 Name (14 characters) (Enter NA to Null)	NLB10	=	______
Clear Local Bit LB10 Label (7 characters) (Enter NA to Null)	CLB10	=	______
Set Local Bit LB10 Label (7 characters) (Enter NA to Null)	SLB10	=	______
Pulse Local Bit LB10 Label (7 characters) (Enter NA to Null)	PLB10	=	______
Local Bit LB11 Name (14 characters) (Enter NA to Null)	NLB11	=	______
Clear Local Bit LB11 Label (7 characters) (Enter NA to Null)	CLB11	=	______
Set Local Bit LB11 Label (7 characters) (Enter NA to Null)	SLB11	=	______
Pulse Local Bit LB11 Label (7 characters) (Enter NA to Null)	PLB11	=	______
Local Bit LB12 Name (14 characters) (Enter NA to Null)	NLB12	=	______
Clear Local Bit LB12 Label (7 characters) (Enter NA to Null)	CLB12	=	______
Set Local Bit LB12 Label (7 characters) (Enter NA to Null)	SLB12	=	______
Pulse Local Bit LB12 Label (7 characters) (Enter NA to Null)	PLB12	=	______
Local Bit LB13 Name (14 characters) (Enter NA to Null)	NLB13	=	______
Clear Local Bit LB13 Label (7 characters) (Enter NA to Null)	CLB13	=	______
Set Local Bit LB13 Label (7 characters) (Enter NA to Null)	SLB13	=	______
Pulse Local Bit LB13 Label (7 characters) (Enter NA to Null)	PLB13	=	______
Local Bit LB14 Name (14 characters) (Enter NA to Null)	NLB14	=	______
Clear Local Bit LB14 Label (7 characters) (Enter NA to Null)	CLB14	=	______

Set Local Bit LB14 Label (7 characters) (Enter NA to Null)	SLB14	=	______
Pulse Local Bit LB14 Label (7 characters) (Enter NA to Null)	PLB14	=	______
Local Bit LB15 Name (14 characters) (Enter NA to Null)	NLB15	=	______
Clear Local Bit LB15 Label (7 characters) (Enter NA to Null)	CLB15	=	______
Set Local Bit LB15 Label (7 characters) (Enter NA to Null)	SLB15	=	______
Pulse Local Bit LB15 Label (7 characters) (Enter NA to Null)	PLB15	=	______
Local Bit LB16 Name (14 characters) (Enter NA to Null)	NLB16	=	______
Clear Local Bit LB16 Label (7 characters) (Enter NA to Null)	CLB16	=	______
Set Local Bit LB16 Label (7 characters) (Enter NA to Null)	SLB16	=	______
Pulse Local Bit LB16 Label (7 characters) (Enter NA to Null)	PLB16	=	______

Trigger Conditions

Trigger SER (24 Relay Word bits per SERn equation, 96 total)

SER1 = ______

SER2 = ______

SER3 = ______

SER4 = ______

Relay Word Bit Aliases

Syntax: ‘Relay-Word Bit’ ‘Up to 15 characters’. Use NA to disable setting.

ALIAS1 = ______

ALIAS2 = ______

ALIAS3 = ______

ALIAS4 = ______

ALIAS5 = ______

ALIAS6 = ______

ALIAS7 = ______

ALIAS8 = ______

ALIAS9 = ______

ALIAS10 = ______

ALIAS11 = ______

ALIAS12 = ______

ALIAS13 = ______

ALIAS14 = ______

ALIAS15 = ______

ALIAS16 = ______

ALIAS17 = ______

ALIAS18 = ______

ALIAS19 = ______

ALIAS20 = ______

Note: RTSCTS setting does not appear if PROTO=LMD or DNP. LMD PREFIX, ADDR, and SETTLE do not appear if PROTO=SEL or DNP. See Appendix C: SEL Distributed Port Switch Protocol (LMD) for details on LMD protocol and see Appendix G: Distributed Network Protocol (DNP) 3.00 for details on DNP protocol.

Port 1 (SET P 1) Rear Panel, EIA-485 plus IRIG-B

Port Protocol (SEL, LMD, DNP, RTDA, RTDB)	PROTO	=	________
LMD Prefix (@, #, $, %, &)	PREFIX	=	________
LMD Address (1–99)	ADDR	=	________
LMD Settling Time (0.00–30.00 seconds)	SETTLE	=	________
Baud (300, 1200, 2400, 4800, 9600, 19200)	SPEED	=	________
Data Bits (7, 8)	BITS	=	________
Parity Odd, Even, or None (O, E, N)	PARITY	=	________
Stop Bits (1, 2)	STOP	=	________
Time-out (for inactivity) (0–30 minutes)	T_OUT	=	________
Send auto messages to port (Y, N)	AUTO	=	________
Enable hardware handshaking (Y, N)	RTSCTS	=	________
Fast Operate Enable (Y, N)	FASTOP	=	________

Port 2 (SET P 2) Rear Panel, EIA-232 with IRIG-B

Port Protocol (SEL, LMD, DNP, RTDA, RTDB)	PROTO	=	________
LMD Prefix (@, #, $, %, &)	PREFIX	=	________
LMD Address (1–99)	ADDR	=	________
LMD Settling Time (0.00–30.00 seconds)	SETTLE	=	________
Baud (300, 1200, 2400, 4800, 9600, 19200)	SPEED	=	________
Data Bits (7, 8)	BITS	=	________
Parity Odd, Even, or None (O, E, N)	PARITY	=	________
Stop Bits (1, 2)	STOP	=	________
Time-out (for inactivity) (0–30 minutes)	T_OUT	=	________
Send auto messages to port (Y, N)	AUTO	=	________
Enable hardware handshaking (Y, N)	RTSCTS	=	________
Fast Operate Enable (Y, N)	FASTOP	=	________

Port 3 (SET P 3) Rear Panel, EIA-232

Port Protocol (SEL, LMD, DNP, RTDA, RTDB)	PROTO	=	________
LMD Prefix (@, #, $, %, &)	PREFIX	=	________
LMD Address (1–99)	ADDR	=	________
LMD Settling Time (0.00–30.00 seconds)	SETTLE	=	________
Baud (300, 1200, 2400, 4800, 9600, 19200)	SPEED	=	________
Data Bits (7, 8)	BITS	=	________
Parity Odd, Even, or None (O, E, N)	PARITY	=	________
Stop Bits (1, 2)	STOP	=	________
Time-out (for inactivity) (0–30 minutes)	T_OUT	=	________
Send auto messages to port (Y, N)	AUTO	=	________
Enable hardware handshaking (Y, N)	RTSCTS	=	

Fast Operate Enable (Y, N)	FASTOP	=	________

Port 4 (SET P 4) Front Panel, EIA-232

Port Protocol (SEL, LMD, DNP, RTDA, RTDB)	PROTO	=	________
LMD Prefix (@, #, $, %, &)	PREFIX	=	________
LMD Address (1–99)	ADDR	=	________
LMD Settling Time (0.00–30.00 seconds)	SETTLE	=	________
Baud (300, 1200, 2400, 4800, 9600, 19200)	SPEED	=	________
Data Bits (7, 8)	BITS	=	________
Parity Odd, Even, or None (O, E, N)	PARITY	=	________
Stop Bits (1, 2)	STOP	=	________
Time-out (for inactivity) (0–30 minutes)	T_OUT	=	________
Send auto messages to port (Y, N)	AUTO	=	________
Enable hardware handshaking (Y, N)	RTSCTS	=	________
Fast Operate Enable (Y, N)	FASTOP	=	________

Port n (SET P n) Front Panel, EIA-232 for PROTO = RTDA

Number of RTDA (0–12)	RTDNUM A	=	________
RTD 1A Type (NA, PT100, NI100, NI120, CU10)	RTD1TA	=	________
RTD 2A Type (NA, PT100, NI100, NI120, CU10)	RTD2TA	=	________
RTD 3A Type (NA, PT100, NI100, NI120, CU10)	RTD3TA	=	________
RTD 4A Type (NA, PT100, NI100, NI120, CU10)	RTD4TA	=	________
RTD 5A Type (NA, PT100, NI100, NI120, CU10)	RTD5TA	=	________
RTD 6A Type (NA, PT100, NI100, NI120, CU10)	RTD6TA	=	________
RTD 7A Type (NA, PT100, NI100, NI120, CU10)	RTD7TA	=	________
RTD 8A Type (NA, PT100, NI100, NI120, CU10)	RTD8TA	=	________
RTD 9A Type (NA, PT100, NI100, NI120, CU10)	RTD9TA	=	________
RTD 10A Type (NA, PT100, NI100, NI120, CU10)	RTD10TA	=	________
RTD 11A Type (NA, PT100, NI100, NI120, CU10)	RTD11TA	=	________
RTD 12A Type (NA, PT100, NI100, NI120, CU10)	RTD12TA	=	________

Port n (SET P n) Front Panel, EIA-232 for PROTO = RTDB

Number of RTDB (0–12)	RTDNUM B	=	________
RTD 1B Type (NA, PT100, NI100, NI120, CU10)	RTD1TB	=	________
RTD 2B Type (NA, PT100, NI100, NI120, CU10)	RTD2TB	=	________
RTD 3B Type (NA, PT100, NI100, NI120, CU10)	RTD3TB	=	________
RTD 4B Type (NA, PT100, NI100, NI120, CU10)	RTD4TB	=	________
RTD 5B Type (NA, PT100, NI100, NI120, CU10)	RTD5TB	=	________
RTD 6B Type (NA, PT100, NI100, NI120, CU10)	RTD6TB	=	________
RTD 7B Type (NA, PT100, NI100, NI120, CU10)	RTD7TB	=	________
RTD 8B Type (NA, PT100, NI100, NI120, CU10)	RTD8TB	=	________
RTD 9B Type (NA, PT100, NI100, NI120, CU10)	RTD9TB	=	________
RTD 10B Type (NA, PT100, NI100, NI120, CU10)	RTD10TB	=	

RTD 11B Type (NA, PT100, NI100, NI120, CU10)	RTD11TB	=	________
RTD 12B Type (NA, PT100, NI100, NI120, CU10)	RTD12TB	=	________

Appendix C- FFT Matlab Script

```
% Function name: Inrush_current_plotting
% Author: Glenn Springall
% Pupose: To determine the harmonics present in an inrush sample
% Date of last edit: 29 October 2008
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%

function Inrush_current_plotting
clear
clc

phaseA=csvread('20080714n1c1.csv')-0.0044; %loads the csv file and
removes the centre error
phaseB=csvread('20080714n1c2.csv'); %loads the csv file
phaseC=csvread('20080714n1c3.csv'); %loads the csv file


New_phaseA=phaseA;
New_phaseB=phaseB;
New_phaseC=phaseC;

%Plot of original waveforms
figure(1)
plot(New_phaseC)
hold on
grid on
plot(New_phaseA,'r')
plot(New_phaseB,'g')
title('Current per phase at energisation')
ylabel('Current (no units)')
xlabel('Sample Number')

%fft of original signal
sigFFTA=fft(New_phaseA);
sigFFTB=fft(New_phaseB);
sigFFTC=fft(New_phaseC);

%subplots of the first
figure(2)
for Q=1:27
        subplot(3,1,1)
    stem(50*Q,((abs(sigFFTA(Q+1)))*(2/1250)))
    hold on
    title('FFT of phase A')
    xlabel('Frequency (Hz)')
    ylabel('Phase A')
        subplot(3,1,2)
    stem(50*Q,((abs(sigFFTB(Q+1)))*(2/1250)))
    hold on
    title('FFT of phase B')
    xlabel('Frequency (Hz)')
    ylabel('Phase B')
```

```
    subplot(3,1,3)
    stem(50*Q,((abs(sigFFTC(Q+1)))*(2*1250)))
    hold on
    title('FFT of phase C')
    xlabel('Frequency (Hz)')
    ylabel('Phase C')
end

%produces a percentage figure of the 2nd harmonic relative to the
%fundamental frequency (50Hz)
percentage_second_harmonic_A=abs(sigFFTA(3)/sigFFTA(2))*100
percentage_second_harmonic_B=abs(sigFFTB(3)/sigFFTB(2))*100
percentage_second_harmonic_C=abs(sigFFTC(3)/sigFFTC(2))*100
```

THIS PAGE IS INTENTIONALLY LEFT BLANK